Novel gallium arsenide monolithic microwave devices and their applications

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NOVEL GALLIUM ARSENIDE MONOLITHIC MICROWAVE DEVICES AND THEIR APPLICATIONS

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To My Mother and Father
and
Melanie

Abstract

Two novel monolithic microwave devices are studied. Firstly, a GaAs MESFET is made wide enough such that distributed coupling effects are observed between the source, gate and drain electrodes. Three devices with different electrode geometries are fabricated and characterized up to 20GHz. Directional coupling is observed between the source and drain electrodes, the directivity of which is tunable with gate bias. High directivity is obtained, comparable with commercially available hybrid designs with the added advantage of voltage control.

A quasi-TEM model for the wide FET is developed which calculates the six-port S-parameters in terms of electrode geometry and intrinsic FET model parameters. Measured and modelled results are compared for the three devices and show good agreement. The model is then used to simulate device performance unaffected by test fixtures and further improvements in performance are predicted.

The wide FET is then used in two further applications. Firstly as a Schiffman-type phase shifter, here source and drain are shorted to form a meandered coupled line section, where variation in the gate bias produces large, continuously variable phase shift. Secondly, two wide FETs are configured as a tandem coupler such that high backward coupling is obtained, this can then be used as the through transmitted path. An integrated design is fabricated and reasonable through transmission with high, tunable directivity is obtained.

The second device is a planar Schottky barrier diode. Two reduced size diodes are fabricated : a narrow diode for low capacitance detector applications and a wider diode for higher capacitance varactor applications. The devices are up to fifty times smaller than a shorted FET design. Both devices are configured as microwave detectors, the narrow diode exhibits good, broadband performance. Five narrow diodes are then integrated as varactors in a loaded-line phase shifter and good, continuously variable, fixed time delay performance is obtained.

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Glossary of Symbols

a	Transistor active layer depth
a_c	Internal incident wave variable
a_p	External incident wave variable
a_i	General incident wave variable
A_{ij}	Travelling wave amplitude
b_c	Internal reflected wave variable
b_p	External reflected wave variable
b_i	General reflected wave variable
C	Lumped capacitance
C_{dep}	Depletion capacitance
C_{ds}	Drain - source capacitance
C_{ij}	Total inter-electrode capacitance
C_{ij}^a	Air-side inter-electrode capacitance
C_{ij}'	Individual inter-electrode capacitance
C_p	Modified depletion capacitance
d.c.	Direct current
E_z	z directed electric field eigenwave
FET	Field effect transistor
f	Frequency
GaAs	Gallium arsenide
g_m	FET transconductance
G_p	Depletion conductance

G_{ds}	Drain - source conductance
h	Finite difference mesh spacing
H	Height
H_z	z directed magnetic field eigenwave
IC	Integrated circuit
I_{ds}	Drain - source current
I_{dss}	Maximum drain - source current
I_x	Total instantaneous current on line x
$[I]$	Matrix of total instantaneous currents
j	$\sqrt{-1}$
K_c	Coupling factor
l	Length
L	Lumped inductance
L_{ij}	Inter-electrode inductance
L_c	Connection inductance
l_g	Gate length
M1	Metal layer 1
M2	Metal layer 2
M3	Metal layer 3
MESFET	Metal semiconductor FET
MOSFET	Metal oxide semiconductor FET
MIC	Microwave integrated circuit
MMIC	Monolithic microwave integrated circuit
MIS	Metal insulator semiconductor

n	Ideality factor
P_x	Power measured at port x
Q	Quality factor
r	Resistor value
r.f.	Radio frequency
r_s	Series resistance
R_d	Drain series resistance
R_{dep}	Depletion resistance
R_{ds}	Drain - source resistance
R_g	Gate series resistance
R_s	Source series resistance
R_n^+	Ohmic contact resistance
R_{vx}	Mode voltage ratio for mode x
$[R_v]$	Matrix of voltage eigenvectors
RNA	Resistance network analogue
S	Spacing
S_{cc}	Scattering matrix for internal ports
S_{cp}	Scattering matrix for internal to external ports
S_{pc}	Scattering matrix for external to internal ports
S_{pp}	Scattering matrix for external ports
S_n	Total external scattering matrix
S_{ij}	Scattering parameter
T_{xk}	Transmission coefficient for mode x on line k
TEM	Transverse electromagnetic

TRL	Thru-reflect-line calibration technique
$[U]$	Unit matrix
v_x	Voltage at mesh-point x
V_{ds}	Drain - source voltage
V_g	Gate voltage
V_{gs}	Gate - source voltage
V_x^+	Incident travelling wave voltage for mode x
V_x^-	Reflected travelling wave voltage for mode x
V_{Tk}^+	Total incident travelling wave voltage at port k
V_{Tk}^-	Total reflected travelling wave voltage at port k
V_p	Pinch-off voltage
V_x	Total instantaneous voltage on line x
$[V]$	Matrix of total instantaneous voltages
VNA	Vector network analyser
W	Width
Y_{dep}	Depletion admittance
Y_{ij}	Admittance parameter
Y_T	Total admittance matrix
Y_{xk}^m	Mode admittance of mode x on line k
$[Y]$	Admittance matrix
Z_{ij}	Impedance parameter
Z_o	Characteristic impedance
Z_{oe}	Even mode impedance
Z_{oo}	Odd mode impedance

Z_{oi}	Terminal impedance at port i
Z_{xk}^{m}	Mode impedance of mode x on line k
$[Z]$	Impedance matrix
β	Lossless propagation constant
γ_i	Complex propagation constant for mode i
Γ	Connection matrix
Γ_{xk}	Reflection coefficient for mode x on line k
Δx	Small increment in x
Δf	Frequency difference
ϵ_o	Free space permittivity
ϵ_r	Dielectric constant
ϵ_{reff}	Effective dielectric constant
Φ_b	Metal to semiconductor barrier height
λ	Eigenvalue
ρ	Charge density
ω	Angular frequency

Chapter 1

Introduction

1.1 The Growth of Microwave Technology

The last sixty years has seen the microwave electronics industry grow into a significant sector of the world electronics market [1], [2]. The initial impetus was the need for the rapid development of radar during the second world war [3], [4]. It was found that the wavelength of microwave radiation was such that practical sized antennas could be built from which highly directional beams could be used to determine target location [5]. In the 1920-30s the development of line-of-sight communication systems was taking place, one of the first systems was demonstrated between Dover and Calais in 1931 [3]. It is well known that the amount of information that can be transmitted by a communication system is proportional to the available bandwidth, thus at microwave frequencies, in the range of 1GHz to 300GHz, large amounts of information can be transmitted [5]. For example in 1948 the TD-2 system was used as part of the Bell network operating between 3.7 and 4.2GHz with 480 voice circuits, by 1974 the TN-1 system had a capacity of 1800 voice circuits [5].

In the 1960s satellite communication began to develop allowing microwave communication between points not in line-of-sight [5]. The first microwave satellite system used the Telestar satellite, launched in 1962, to transmit live television pictures from the U.S. to Europe. In the

1980s direct broadcast satellite systems [6] were developed allowing television reception over large areas using parabolic antennas with diameters of three feet, operating around 11GHz. Finally today there are a myriad of microwave applications ranging from vehicle collision avoidance radar [7], in-car navigation systems [7] to phased array electronically-steerable radar [8].

1.2 The Development of GaAs Monolithic Microwave Integrated Circuits

One of the main features of the growth in microwave electronics, as was witnessed in digital electronics, was the constant reduction in circuit size and increase in circuit through-put, leading to dramatic reductions in unit costs [9]. The first microwave systems used two-wire, and coaxial transmission lines, later, hollow pipe waveguides [3], [4] came in to use. Waveguides could carry hundreds of watts to an antenna with very little loss and were used extensively in radar systems. Waveguides are still popular today as means of transmitting very high powers, however, on the receiver side, where the powers are much lower, different transmission technologies could be employed. One of the first reduced size transmission line technologies was a flat strip coaxial transmission line used by Rumsey and Jamieson discussed by Barret [10]. This evolved into the microwave printed circuit as reported by Barret and Barnes [11]. Soon after this Greig and Engelmann [12] announced the Microstrip, which used a thin strip conductor supported on a dielectric substrate above a ground plane. Using this structure, components that previously had dimensions of the order of centimetres were reduced to millimetres, thus components such as couplers, filters and antennas could be designed on a very small scale.

Around the same time as these reduced size microwave circuits were being produced the bipolar transistor first proposed by Shockley in 1949 [13] and later the field effect transistor [14] were in production and available in chip form, which was compatible with the microstrip transmission medium. This led to the development of the microwave integrated

circuit (MIC), where semiconductors are mounted upon the microstrip substrate together with passive components to form microwave modules with much reduced size compared to their waveguide or coaxial counterparts [15]. By the mid-1960s complex transmit-recieve modules were being produced for phased array applications by companies such as Texas Instruments under the MERA (Molecular Electronics for Radar Applications) initiative [15]. By 1968 over 600 S-band phased array modules had been produced by Texas Instruments, in what is believed to be the first time MICs had been made in such quantities [15].

The MERA initiative had grown from ideas first postulated by Von Hippel [16] in the early 1950s, concerning molecular engineering. The idea of an electronic circuit as a solid block was also postulated by Dummer [17]. Von Hippel [16] suggested that materials should be designed to perform specific functions, rather than use standard materials and states : "... we can dream up completely new devices". These ideas led the U.S. Air Force to define a new technology termed Molecular Electronics, which eventually spawned the MERA program.

The MERA program led a number of workers to patent devices to be used as part of a radar system including mixers, phase shifters and amplifiers [15]. The key feature of these devices being that both semiconductors devices and passive components such as transmission lines were integrated on the same substrate. The term monolithic, meaning "one rock" became used for these type of circuits, in which the whole circuit was fabricated using one process and the term monolithic microwave integrated circuit (MMIC) began to be used [15]. Of these workers Hytlin studied the properties of the microstrip line on a silicon substrate [18] and a number of silicon MMICs were developed. However, these circuits were plagued by problems associated with the low resistivity of the processed silicon substrates.

Gallium arsenide (GaAs) had been suggested as a material for depositing germanium upon to form transistors, since the GaAs transistor was proving to be a problem [19]. Hytlin filed a patent in 1966 for a MMIC containing a Gunn oscillator, transmission lines and a balanced mixer all integrated on GaAs [19]. The key development, however, in the use of GaAs MMICs was the Schottky barrier MESFET. Around 1966 this device was being

developed by a number of workers, Mead et al [20], Turner et al [21] and workers at IBM Zurich. The device eventually yielded 6dB gain at 10GHz [19]. Thus all the elements were in place to fabricate GaAs MMICs, however, it was not until 1976 that Pengelly and Turner [22] reported the first X-band fully monolithic amplifier.

The following years witnessed a rapid growth in the GaAs MMICs market where, for example, hundreds of identical chips were used in phased array applications [19]. In 1984 Plessey Caswell set up the first GaAs IC foundry solely devoted to analogue ICs [21], it is this foundry that is used for the fabrication of devices studied in this work. In more recent years large U.S. military programs such as MIMIC (Microwave and Millimetre Wave Integrated Circuits) [23] have realized, high performance, repeatable and affordable GaAs MMICs in large volumes.

1.3 Devices Studied

In this work two types of monolithic device are investigated. Firstly, three very wide ($\simeq$1.5mm) GaAs MESFETs are configured as six-ports where the source, gate, and drain electrodes are considered as coupled microstrip transmission lines. The FETs are wide enough such that distributed coupling effects can be observed between the electrodes. It is found that directional coupling is exhibited and the characteristics of the directional coupler can be controlled by the applied gate bias.

Secondly, two planar Schottky barrier diodes are fabricated using standard foundry techniques. The two devices have different junction widths, one device has a wide junction, $\simeq$115μm, for use in varactor applications and the other has a narrow junction, $\simeq$19μm, for low capacitance detector applications.

All devices studied have been fabricated at GEC Marconi Materials Technology Ltd (GMMT), Towcester, UK, through a SERC initiative and a Eurochip quota award. The initial devices where designed using the GMMT F14 process, later devices used the F20 process. The differences between these processes are the introduction of through substrate vias and a reduction of gate length from 0.7μm to 0.5μm in the F20 process. This gives usable FET performance to 20GHz.

A detailed description of the process is given in the foundry design guide [24], a brief description of the main features will be given here. The F20 process is a 14 layer, ion-implanted process, on 200μm gallium arsenide. The process uses three metal layers : metal 1 (M1) defines ohmic contacts, metal 2 (M2) defines Schottky barrier contacts for the FET gates and is used as a first level interconnect, metal 3 (M3) defines the second layer interconnects. M2 and M3 layers are separated by two dielectric layers, Nitride and Polyimide, allowing the formation of metal-insulator-metal (MIM) capacitors. Spiral inductors are defined in M3 with an M2 underpass. Resistors are defined by making ohmic contacts to ion implanted regions. Finally the whole circuit is passivated with a second nitride layer. Using this process all standard lumped elements and transmission lines, together with FETs can be defined, allowing the design of MMICs to 20GHz.

1.4 Motivation for This Work

The description above illustrates the very flexible environment which the MMIC process offers the microwave engineer. The engineer is no longer constrained to one metal layer interconnecting discrete devices, but can create multilevel designs, for example, the stacked spiral inductor, where both M2 and M3 layers are spiralled to give very high inductance values [24] or thin film microstrip [25], where M2 is used as a ground plane for M3 to create very low impedance microstrip lines. In this work the availability of a Schottky contact layer is used to combine standard passive devices with active devices to create new, tunable monolithic microwave devices. Tunability is a great asset for monolithic devices since post-

fabrication tuning or "tweaking", once an essential art for the microwave engineer, is virtually impossible with standard MMICs. Other workers have used similar ideas to fabricate tunable phase shifters [26] and attenuators [27].

The monolithic microwave process is opening up new horizons to the microwave engineer, beyond merely transferring standard lumped circuits onto GaAs but in the words of Von Hippel, used in the 1950s at the inception of monolithic circuits : " No longer shackled by available materials and empirical performance characteristics, we can dream up completely new devices".

1.5 Thesis Structure

Chapter 2 of this thesis reviews methods for analysing wide FET structures. A quasi-TEM model for a wide FET structure is developed, allowing the six-port S-parameters to be calculated in terms of the wide FET electrode geometries and the intrinsic FET model parameters. A number of improvements are introduced to the model and measurement test fixture parasitics are also included.

Chapter 3 discusses a number of measurement issues relating to the measurement of active multiport devices. Included are multiport device measurements using a two-port network analyser, biasing of active devices, on-wafer probing and the evaluation of the measurement test fixtures.

Chapter 4 presents detailed measurements and modelling of an initial wide FET structure, configured as a four and six-port directional coupler. The three coupled microstrip line analysis used as a basis for the wide FET model is validated by comparison with other workers' data and is compared with measured data for passive three coupled microstrip lines. The wide FET structure is then fully characterized using preliminary test fixtures. Measurements using improved test fixtures are then shown and these are compared to modelled results. Six-

port measurements are then presented and these lead to improvements in the model. The wide FET structure is shown to exhibit backward coupling between source and drain lines, the directivity of which can be controlled by the d.c. gate bias, resulting a tunable directivity coupler.

In chapter 5 two further wide FETs with different electrode geometries are characterized and measured and modelled results are shown and compared with the initial FET design. Finally, further improvements to the model are implemented and measured and modelled results are shown for all three wide FET structures. The model is then used to simulate the performance of the wide FETs with low inductance connections and high, tunable directivities are predicted.

Chapter 6 presents two further applications using a wide FET as the basic element. Firstly, the model developed in chapter 2 is used to predict the device performance when configured as a phase shifter and reasonable performance is predicted. A wide FET is then configured as a phase shifter and the measured and modelled results show reasonable agreement. Secondly, the model is used to predict the performance of two wide FETs connected as a tandem directional coupler so as to increase the through transmission of the coupler. Two FETs are then configured in tandem and improved through transmission is observed. A fully integrated design is then carried out with two wide FETs on one chip and reasonable performance is obtained.

Chapter 7 presents results for two planar Schottky barrier diodes with different junction widths. One device has a wide junction $\simeq 115\mu$m for varactor applications and the other has a narrow junction $\simeq 19\mu$m for low capacitance detector applications. The diodes are characterized at d.c. and microwave frequencies. The narrow and wide diodes are modelled using a simple diode model to obtain estimates of the junction capacitance. Both diodes are then configured as detectors, their performance is compared and the narrow diode is shown to exhibit good detector performance. An integrated loaded-line phase shifter is then designed and fabricated using five narrow diodes in parallel. The measured results show

good fixed time delay performance, ideal for phased array applications.

Finally chapter 8 presents the conclusions of this work and suggests future work and other possible applications for the devices studied.

Chapter 2

Theoretical Analysis of a Wide FET

2.1 Introduction and Review of Related Work

Wide FETs have been of interest for many years. Initial interest was in Travelling Wave FETs (TWFs) [28], where a FET structure is made wide enough such that a growing wave can propagate along the device producing very broadband gain. Although this work is not concerned directly with these devices, it is useful to discuss them since they show the possible forms of analysis available for the general wide FET structure. The main differences between a TWF analysis and the analysis required in this work is that the FET will not be biased in the drain-source sense, thus no current source will be present in the output and that the source is not grounded, thus a full three-line analysis is required. Other workers have analysed wide FET-type structures [27, 29] that have application as variable attenuators and phase shifters, but these are in coplanar configurations where the source and drain contacts are considered as being grounded. Wide FETs with dual gates have also been analysed as coupled coplanar lines for voltage variable coupling applications, again with source and drain considered grounded [30, 31]. To the author's knowledge this work is the first analysis of a wide FET structure in a "switching" type of configuration, where neither source nor drain are grounded and no drain-source bias is present. The analyses discussed here fall into two

broad categories : quasi-TEM analysis and full wave analysis, this work uses a quasi-TEM analysis, thus the merits of the two approaches will be discussed, and reasons for the choice of analysis technique will be given.

One of the first quasi-TEM analyses was carried out by McIver [28]. Here a distributed model of a MOSFET structure is used with input and output transmission lines having inductance and capacitance per unit length. The lines are coupled by a distributed current source. The voltage and currents on the output line are then found by integrating along the device. A set of differential equations can then be obtained, relating output current to input voltage, hence the gain of the device can be obtained. A more complete analysis of a true MESFET structure is given by Podgorski [32]. Here voltage Green's functions are used to solve for the voltage and current on the output transmission line in terms of the distributed, dependent current sources on the output line. An alternative analysis is performed by Wei [33] on a different TWF structure. A coupled mode method is used where a pair of coupled differential equations are obtained for the voltage on the gate and drain lines. Boundary conditions at the line terminations are then imposed and the gate and drain voltages can be obtained in terms of transmission line constants and distance along the device. A complete three-line structure analysis was carried out by Holden *et al* [34]. Firstly the inter-electrode capacitances for the three-line system are calculated using a Green's function method, from these passive, distributed admittance and impedance matrices can be derived. An active admittance matrix for the device is then obtained by calculating the admittance parameters of the standard FET model in terms of the three electrodes. The passive and active admittance matrices can then be added to give a complete model for the device. Kirchoff's voltage and current laws are then applied to a small element of line Δx and transmission line equations relating voltages and currents on all three lines are obtained. These equations are combined to solve for voltage and current, they show that three possible modes can exist on the structure. Knowledge of the voltage and current on the lines then leads to calculations of the scattering parameters for the device. A similar analysis technique is used by D'Agostino *et al* [35]. The capacitance matrix is calculated using the moment method [36]. The standard transmission line equations are solved using Laplace transforms

and the scattering parameters are obtained from the open-circuit impedance matrix.

Although these quasi-TEM analyses give reasonable results, the limitations of the techniques must be considered. The wide FET is essentially a microstrip coupled line structure and because the metallic conductor is supported by a dielectric, the medium of the transmission line is inhomogeneous. At the air-dielectric interface, because of field continuity, components of electric and magnetic field exist in the direction of propagation, thus TEM propagation no longer exists. The quasi-TEM approximation assumes these components to be small compared to those that exist beneath the conductor, full wave analyses have shown this to be a reasonable assumption [37]. The non-TEM propagation on microstrip also leads to dispersion where the propagation constant and characteristic impedance vary with frequency, thus at high frequencies ($>$ 10GHz) dispersion models may be required to improve the quasi-TEM model [37].

The other main approximation of quasi-TEM analyses is that the cross-sectional dimensions of the transmission line structure are small compared with the propagating wavelength [37], if this is the case the fields can be assumed to be those of the static, non-time varying case, commonly referred to as the quasi-static approximation. Since this work deals almost exclusively with monolithic structures, where the cross-sectional dimensions are extremely small, this is a reasonable assumption. Another major limitation to the quasi-TEM approximation is that of higher order modes. Above a certain frequency the microstrip structure can support waveguide modes and surface modes, whose propagation characteristics are radically different from quasi-TEM. Above the cut-off frequencies of these modes power can be coupled into these modes, especially when discontinuities are present, resulting in non-quasi-TEM behaviour. Microstrip structures are generally operated below the cut-off of these modes, expressions for the cut-off frequencies are given by Gupta *et al* [37]. Higher order modes occur when the dimensions of the cross-section of the transmission line structure are no longer small compared to the propagating wavelength, since the quasi-static approximation is valid for the structures analysed in this work, the effect of higher order modes should be minimal. Another effect not accounted for by a quasi-TEM analysis is that of skin depth. This is where

as the frequency increases, the current flowing in a transmission line is no longer distributed evenly across the conductors, the current tends to concentrate at the surface producing an increase in effective resistance [5]. At microwave frequencies the skin depth can be very small, for example, with gold at 10GHz the skin depth is 0.79μm [38]. The skin effect can be included in a quasi-TEM analysis by giving the series resistance of the transmission line the appropriate relationship with frequency.

Full wave analyses are much more rigorous, they can calculate the fields for all the possible modes of the structure and account for dispersion effects. One of the first full wave analysis of a FET structure was carried out by Heinrich [39]. A mode-matching technique is used [40], in this analysis the FET structure is divided up into a number of regions and the electric and magnetic fields are represented in each of the regions as infinite sums of their eigenfunctions [41] with unknown coefficients. Each eigenfunction represents an H_z or E_z eigenwave. Boundary conditions are then introduced and an infinitely homogeneous system of equations is produced, the solution of which yields the propagation constants for the structure.

Although a full-wave approach would yield very accurate results, it requires detailed knowledge of the structure, doping levels and conductivities of the FET, these are not easily obtainable from competition conscious manufacturers. FET data is more commonly available in terms of equivalent circuit models which immediately points to the use of quasi-TEM analyses. Indeed, Heinrich himself goes on to published an equivalent circuit analysis [42] based on the full-wave analysis as a more practical approach. Thus, initially a quasi-TEM approach was taken, if this proved to be inaccurate or unable to model the device adequately, a more detailed approach would be investigated.

In this chapter a model for the wide FET structure is developed. The analysis is based on the work of Holden *et al* [34], combined with two and three line analyses by Tripathi [43, 44, 45, 46, 47] and Gunton *et al* [48], this chapter shows in detail how the full six-port, arbitrarily terminated, S-parameters for a wide FET structure are obtained from the electrode geometries and the intrinsic FET model parameters.

Firstly, the six-port S-parameters of a symmetrical three coupled line system are derived solely from its transmission line parameters : the series impedance and shunt admittance matrices (immittance parameters). Thus to model the complete wide FET structure we are required to find its immittance parameters. These are found from a combination of the passive, coupled line immittance parameters for the FET electrodes and the admittance matrix obtained from the lumped element FET model. It is well known that the lossless, passive coupled line immittance parameters can obtained from the inter-electrode capacitances of the system [49], with and without dielectric, these will be calculated using the resistive network analogue technique [50], [51]. This method will be described and compared with other possible techniques. The equivalent circuit used to model the intrinsic FET will then be discussed, initially a basic model is proposed, a number of modifications are later introduced to give an improved model. The admittance parameters for the intrinsic FET are then derived and assumptions made in the derivation are discussed. Finally a method for the inclusion of the effect of external parasitics, introduced by the MMIC test fixture will be presented, a number of other methods will also be described and the relative merits of each discussed.

2.2 Analysis of Three Coupled Lines

This analysis uses a coupled mode method [43, 44, 45], where propagation on the structure is described in terms of modes. For a system of N conductors, N-1 modes are found to exist, each with its own characteristic field distribution. The type of equations that describe these modes and which will be developed in this section are used throughout engineering mathematics, the solutions obtained here are known as the *normal modes* [41] because the eigenvectors that represent the field distributions are orthogonal or normal to each other. All possible solutions can be found from linear combinations of the normal modes.

The system of coupled transmission lines is modelled in terms of their distributed, self and mutual capacitances and inductances (immittance parameters) per unit length, in the lossless case. The standard telegraphers equations are then derived by applying Kirchoff's laws to a vanishingly short length of the coupled transmission lines. The total voltages and currents at any point on the lines are then obtained in terms of the immitances parameters. From these equations, the propagation characteristics of each of the modes can be found. The propagation characteristics are known as the *normal mode parameters* [43, 44], they include the propagation constant of the mode and they will be described in detail in this section. Using the normal mode parameters, the propagation characteristics for each of the modes on each of the lines can be described as if it were a decoupled transmission line. Reflection and transmission coefficients can then be defined for each of the modes on each of the lines and from these the S-parameters can be obtained.

A system of three coupled lines is shown in figure 2.1.

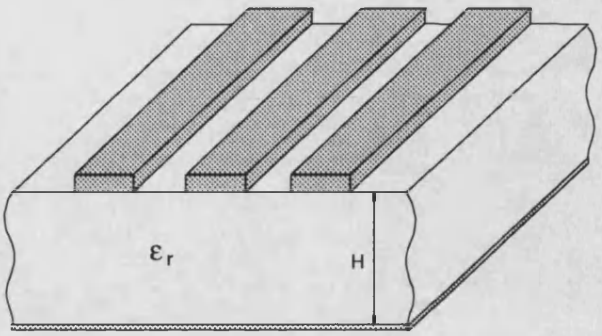

Figure 2.1: Three coupled microstrip lines

The telegraphers equations [37] are found to be

$$\begin{aligned} -\tfrac{dV_1}{dz} &= Z_{11}I_1 + Z_{12}I_2 + Z_{13}I_3 \\ -\tfrac{dV_2}{dz} &= Z_{21}I_1 + Z_{22}I_2 + Z_{23}I_3 \\ -\tfrac{dV_3}{dz} &= Z_{31}I_1 + Z_{32}I_2 + Z_{33}I_3 \end{aligned} \tag{2.1}$$

Where V_i and I_i are the total instantaneous voltage and current at any point on line i and where the Z_{ij} are the self and mutual impedances per metre and in the lossless case

$$Z_{ij} = j\omega L_{ij} \tag{2.2}$$

Where the L_{ij} are the self and mutual inductances per metre.

This can be written in matrix form

$$-\frac{d[V]}{dz} = [Z][I] \tag{2.3}$$

A similar expression can be written for the currents

$$-\frac{d[I]}{dz} = [Y][V] \tag{2.4}$$

Where the Y_{ij} are the self and mutual admittances per metre and in the lossless case

$$Y_{ij} = j\omega C_{ij} \tag{2.5}$$

Where the C_{ij} are the self and mutual capacitances per metre.

If equation 2.3 is differentiated with respect to z and the result substituted in equation 2.4, equation 2.6 is obtained

$$\frac{d^2[V]}{dz} = [Z][Y][V] \tag{2.6}$$

If the form of V_i is assumed to be $V = V_0 e^{-\gamma z}$ - a standard solution to this type of problem, where γ is known as the propagation constant for the line, then equation 2.7 follows

$$\gamma^2[V] = [Z][Y][V] \tag{2.7}$$

Defining

$$\gamma^2 = \lambda \tag{2.8}$$

And

$$[Z][Y] = [P] \tag{2.9}$$

Then equation 2.7 becomes

$$\lambda[V] = [P][V] \tag{2.10}$$

And rearranging

$$([P] - \lambda[U])[V] = 0 \tag{2.11}$$

Where $[U]$ is the identity matrix which is a matrix of the same order as $[P]$ but with all elements equal to zero except for the leading diagonal which are equal to one.

This is a standard form known as an *eigenvalue problem* and requires the solution of a set of linear simultaneous equations in V. If there are i equations it can be shown that there are i values of λ for which equation 2.11 holds, these are known as the *eigenvalues* . In this case the eigenvalues have physical significance : equation 2.8 shows that they are in fact the square of the propagation constants, γ_i. Thus the three different eigenvalues produce three different propagation constants for the set of lines in figure 2.1 . This leads to the idea that there are three different *modes* of propagation for the lines, these will be denoted a, b, c. Mode a is an odd mode, mode b is an even mode and mode c is termed a bulk mode since the voltage distribution is relatively constant across the whole or bulk of the structure. For the case of three equal width lines the voltage distributions of the modes are shown schematically in figure 2.2.

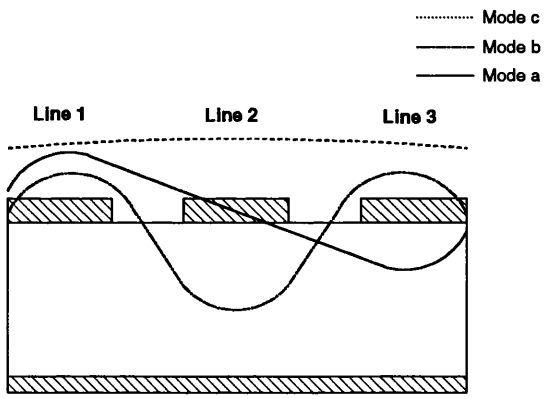

Figure 2.2: Voltage distributions for the three modes on three equal width microstrip lines

If the λ_i are substituted back into equation 2.11, then what are known as the *eigenvectors* of equation 2.11 are obtained and these in fact show the voltages that exist on the three lines for each of the γ_i. These eigenvectors represent the field distributions across the three lines for each of the possible *modes* that can propagate.

Thus the initial task is to find the eigenvalues and eigenvectors. The procedure for this is given in [52] and basically requires the solution of

$$DET([P] - \lambda[U]) = 0 \tag{2.12}$$

Where DET means the determinant of a matrix. Equation 2.12 is known as the *Characteristic Equation.* This type of equation can be solved relatively easily using standard computer routines.

From these eigenvalues, eigenvectors are obtained which are the voltage solutions for each of the modes and it can be shown that they have forward and backward wave components. The total voltage on line 1 of the system, obtained by superimposing the three modes, is

$$V_1 = A_{1a}e^{-\gamma_a z} + A_{2a}e^{+\gamma_a z} + A_{1b}e^{-\gamma_b z} + A_{2b}e^{+\gamma_b z} + A_{1c}e^{-\gamma_c z} + A_{2c}e^{+\gamma_c z} \tag{2.13}$$

Where the A_{1x} and A_{2x} are the voltage amplitudes of the forward and backward waves of mode x respectively.

The eigenvectors from equation 2.11 interrelate the mode voltages on each of the lines, if they are normalized with respect to the mode voltages of line 1 , the total voltages for the three lines can be written in matrix form

$$[V] = [R_v][[A_1] + [A_2]] \tag{2.14}$$

where

$$[[A_1] + [A_2]] = \begin{pmatrix} A_{1a}e^{-\gamma_a z} + A_{2a}e^{+\gamma_a z} \\ A_{1b}e^{-\gamma_b z} + A_{2b}e^{+\gamma_b z} \\ A_{1c}e^{-\gamma_c z} + A_{2c}e^{+\gamma_c z} \end{pmatrix} \tag{2.15}$$

And where $[V]$ is the 3 x 1 matrix of total voltages and $[R_v]$ is the 3 x 3 matrix of normalized eigenvectors, for the case of symmetrical lines, (width line 1 = width line 3) they are found to be

$$[R_v] = \begin{bmatrix} 1 & 1 & 1 \\ 0 & R_{vb} & R_{vc} \\ -1 & 1 & 1 \end{bmatrix} \tag{2.16}$$

where R_{vb} and R_{vc} are the ratios of the mode voltages on line 2 to lines 1 and 3 (mode voltage ratios).

Defining mode admittance as the ratio of mode current to mode voltage and

$$[A_1 - A_2]_x = A_{1x}e^{-\gamma_x z} - A_{2x}e^{+\gamma_x z} \tag{2.17}$$

It follows that

$$\begin{aligned} I_1 &= Y^m_{a1}[A_1 - A_2]_a + Y^m_{b1}[A_1 - A_2]_b + Y^m_{c1}[A_1 - A_2]_c \\ I_2 &= R_{vb}Y^m_{b2}[A_1 - A_2]_b + R_{vc}Y^m_{c2}[A_1 - A_2]_c \\ I_3 &= -Y^m_{a3}[A_1 - A_2]_a + Y^m_{b3}[A_1 - A_2]_b + Y^m_{c3}[A_1 - A_2]_c \end{aligned} \tag{2.18}$$

And in matrix form

$$[I] = [[R_v] \bullet [Y^m]][[A_1] - [A_2]] \tag{2.19}$$

Where $[I]$ is the 3 x 1 matrix of total currents, $[Y^m]$ is the 3 x 3 matrix of mode admittances, $[A_1]$ and $[A_2]$ are the 3 x 1 matrices of voltage mode amplitudes, the negative sign of the backward wave is required if this is to be a solution of equations 1 and 2 ($\bullet$ implies multiplication of the individual elements of the matrix, i.e. if $[c] = [a] \bullet [b]$, then $c_{11} = a_{11} * b_{11}$). If equation 2.19 is differentiated with respect to z then we obtain

$$\frac{d[I]}{dz} = -[[R_v] * [Y^m]][\gamma][A_1 + A_2] \tag{2.20}$$

where $[\gamma]$ is the 3 x 3 diagonal matrix of propagation constants.

If equations 2.20 and 2.14 are substituted in 2.4, equation 2.21 is obtained

$$[R_v] * [Y^m][\gamma] = [Y] * [R_v] \tag{2.21}$$

Expressions for $[Y^m]_{ij}$ can now be written, and since each mode on each line is now expressed independently, not in the coupled form of equation 2.7, the mode impedance is simply the inverse of the mode admittance, $[Z^m]_{ij} = 1/[Y^m]_{ij}$, the expressions are given here

$$\begin{aligned}
Z^m_{a1} &= Z^m_{a3} = \frac{\gamma_a}{Y_{11}-Y_{13}} \\
Z^m_{b1} &= Z^m_{b3} = \frac{\gamma_b}{Y_{11}+Y_{13}+R_{vb}Y_{12}} \\
Z^m_{b2} &= \frac{\gamma_b R_{vb}}{2Y_{12}+R_{vb}Y_{22}} \\
Z^m_{c1} &= Z^m_{c3} = \frac{\gamma_c}{Y_{11}+Y_{13}+R_{vc}Y_{12}} \\
Z^m_{c2} &= \frac{\gamma_c R_{vc}}{2Y_{12}+R_{vc}Y_{22}}
\end{aligned} \tag{2.22}$$

The normal mode parameters for three coupled symmetrical lines have been derived in terms of the transmission line parameters, they are : the propagation constants, the mode impedances and the mode voltage ratios. Each of the lines can be regarded as a decoupled transmission line, propagating three different modes, the amplitudes of which are defined by the normalized eigenvectors. Thus reflection and transmission coefficients for each of the modes on each of the lines can be derived [53] as

$$\Gamma_{xk} = \frac{(\frac{Z^m_{xk}}{Z_k} - \frac{Z_k}{Z^m_{xk}})sinh(\gamma_x l)}{2cosh(\gamma_x l) + (\frac{Z^m_{xk}}{Z_k} + \frac{Z_k}{Z^m_{xk}})sinh(\gamma_x l)} \tag{2.23}$$

$$T_{xk} = \frac{2}{2cosh(\gamma_x l) + (\frac{Z^m_{xk}}{Z_k} + \frac{Z_k}{Z^m_{xk}})sinh(\gamma_x l)} \tag{2.24}$$

Where x denotes the mode, a, b or c; k, line 1, 2 or 3; Z^m_{xk}, the mode impedance and Z_k the line terminating impedance.

It can be shown [44] that the ratio of the mode impedances for lines 1 and 2 or 2 and 3 is a constant for each of the modes, the relationship is shown here

$$\frac{Z_{b2}}{Z_{b1}} = \frac{Z_{c2}}{Z_{c1}} = \frac{-R_{vb}R_{vc}}{2} \tag{2.25}$$

For the symmetrical case, a mode impedance for mode a, the odd mode, is undefined on line 2 because there is a zero of both mode current and mode voltage on this line. This constant impedance ratio for both modes allows the choice of terminating impedances which greatly simplifies the analysis. Gunton and Paige [48] introduced this concept known as non-mode-converting terminations. If the terminating impedances are chosen in this constant ratio it can be readily shown that the reflection coefficients for one mode are the same for each of the lines, using the above notation

$$\Gamma_{x1} = \Gamma_{x2} = \Gamma_{x3} \tag{2.26}$$

This implies that when a mode propagating on the structure is incident upon the line terminations the reflected wave is of the same mode, i.e. no mode conversion occurs. Thus with these terminations only the normal modes of the structure will be present.

A modal analysis can now be used to find the S-parameters of the system. S-parameters (Scattering parameters) are defined in terms of power waves [53, 54], which are the standard travelling voltage and current waves used in transmission line analysis, but normalized to square root of the port impedance. They are most useful in microwave circuit analysis, where power transmission is of the utmost importance and open and short circuits used in the definition of other circuit parameters are difficult to realize.

For this modal analysis unity voltage wave is imposed on port 1 of the device. A unity voltage wave is realized by a linear combination of the normal modes. This linear combination is then imposed on the structure and since the reflection and transmission coefficients for each of the modes on each of the lines has been defined, the scattering parameters for the structure can be obtained. Thus initially the linear combination of the normal modes to give unity voltage wave at port 1 is calculated. Defining the incident and reflected voltage waves of mode x as V_x^+ and V_x^-, respectively, defining the total incident voltage wave at port k as V_{Tk}^+ and using the normalized eigenvectors from equation 2.16, the voltage waves incident on the three ports can be written as

$$V_{T1}^+ = V_a^+ + V_b^+ + V_c^+ \tag{2.27}$$

$$V_{T2}^+ = R_{vb}V_b^+ + R_{vc}V_c^+ \tag{2.28}$$

$$V_{T3}^+ = -V_a^+ + V_b^+ + V_c^+ \tag{2.29}$$

Setting $V_{T1}^+ = 1$ and $V_{T2}^+ = V_{T3}^+ = 0$, gives $V_a^+ = \frac{1}{2}$ and

$$V_b^+ = \frac{-R_{vc}V_c^+}{R_{vb}} \tag{2.30}$$

Substituting in equation 2.27

$$V_c^+ = \frac{R_{vb}}{2(R_{vb} - R_{vc})} \tag{2.31}$$

$$V_b^+ = \frac{-R_{vc}}{2(R_{vb} - R_{vc})} \tag{2.32}$$

Using the reflection coefficients from equation 2.23, the reflected voltage wave for ports 1 and 2 are

$$V_{T1}^- = \frac{\Gamma_a}{2} - \frac{R_{vc}}{2(R_{vb} - R_{vc})}\Gamma_b + \frac{R_{vb}}{2(R_{vb} - R_{vc})}\Gamma_c \tag{2.33}$$

$$V_{T2}^- = -\frac{R_{vb}R_{vc}}{2(R_{vb} - R_{vc})}\Gamma_b + \frac{R_{vc}R_{vb}}{2(R_{vb} - R_{vc})}\Gamma_c \tag{2.34}$$

The definition of an incident power wave at port i is [53]

$$a_i = \frac{V_i^+}{\sqrt{Z_{oi}}} \tag{2.35}$$

and for the reflected power wave

$$b_i = \frac{V_i^-}{\sqrt{Z_{oi}}} \tag{2.36}$$

Where Z_{oi} is the impedance 'seen' looking out of port i.

Scattering parameters are defined as [54]

$$S_{ij} = \frac{b_i}{a_j} \tag{2.37}$$

Thus for S_{11}, since $V_{T1}^{+} = 1$, equation 2.38 follows

$$S_{11} = \frac{\Gamma_a}{2} - \frac{R_{vc}}{2(R_{vb} - R_{vc})}\Gamma_b + \frac{R_{vb}}{2(R_{vb} - R_{vc})}\Gamma_c \tag{2.38}$$

However for S_{21} since $Z_{o1} \neq Z_{o2}$, equation 2.39 is obtained

$$S_{21} = (-\frac{R_{vb}R_{vc}}{2(R_{vb} - R_{vc})}\Gamma_b + \frac{R_{vc}R_{vb}}{2(R_{vb} - R_{vc})}\Gamma_c)\sqrt{\frac{Z_{o1}}{Z_{o2}}} \tag{2.39}$$

Remembering that non-mode-converting terminations have been used and that

$$\frac{Z_{o1}}{Z_{o2}} = -\frac{2}{R_{vb}R_{vc}} \tag{2.40}$$

Equation 2.41 can be written

$$S_{21} = (\Gamma_b - \Gamma_c)\sqrt{\frac{-R_{vb}R_{vc}}{2}}\frac{1}{(R_{vb} - R_{vc})} \tag{2.41}$$

The remaining S-parameters are defined in a similar manner and are given in appendix B.

The S-parameters for the three-line symmetrical case have been defined for the case of non-mode converting terminations. These need to be redefined in terms of the more usual 50Ω

terminations. This is achieved using an impedance renormalization procedure outlined by Tripathi [46].

Thus the S-parameters for three coupled symmetrical transmission lines with arbitrary terminations have been derived from the distributed impedance and admittance matrices for the structure. This analysis is for the general lossy case which results in complex normal mode parameters, thus the FET intrinsic resistances and electrode series resistances can be included in the derivation of the distributed immittance parameters.

In the next section the method used for calculating the immittance parameters of three passive coupled microstrip lines will be shown.

2.3 The Distributed Immittance Matrices for Three Coupled Microstrips

2.3.1 Introduction

In the previous section the S-parameters for the general symmetrical three-line system were derived from the distributed admittance and impedance (immittance) matrices for the structure. In this section methods for the calculation of these matrices will be assessed and the chosen method described in detail.

This section will deal solely with the lossless case, the addition of resistive losses will be discussed in later sections. Since this is the lossless case, equation 2.5 shows that the admittance matrix is completely defined by the capacitance matrix for the conductor system. Under the quasi-TEM approximation it well known [49] that the inductance matrix and hence the impedance matrix can be found from the capacitance matrix with the dielectric removed from the structure. Thus the passive coupled line system is completely characterized by the with and without dielectric capacitance matrices. It should be noted that the capacitances in the matrix of equation 2.5 are total capacitances, that is

$$\begin{aligned} C_{11} &= C'_{11} + C'_{21} + C'_{31} \\ C_{22} &= C'_{22} + C'_{21} + C'_{23} \\ C_{21} &= -C'_{21} \end{aligned} \tag{2.42}$$

Where the C'_{ij} are the individual inter-electrode capacitances. The other capacitances follow in a similar manner. The first method discussed below calculates individual capacitances whereas the following two methods find the total capacitances.

There are a number of approaches that can be adopted for the calculation of inter-electrode capacitances that range from closed form expressions derived from purely analytical techniques such as conformal mapping [55, 37] which can be evaluated easily and quickly using personal computers, through finite difference techniques [56, 57] which require large amounts of computing power and storage, to more efficient numerical techniques such as the spectral

domain method [58].

The closed form approach has not been explicitly derived for three coupled microstrip lines to the authors' knowledge. Mohammed [31] has analysed three coplanar strips, but with no ground plane present. This approach required the combination of single line, and asymmetrical line results, together with some approximations in order to calculate the capacitances simliar to that taken in [59]. One of the main drawbacks of this method was that expressions for the characteristic impedance of the individual lines were required, again closed form expressions were used, however the dimensions of the wide FET structure tended to be outside the range of reasonable accuracy, especially for the very short gate line. A number of approximations were required. Firstly when dealing with asymmetrical lines, the capacitance was obtained by taking the geometric mean of the capacitance for the two different widths. Also, in extending the two line expressions to three lines, no interaction of the central line with the capacitance between the outer lines had to be assumed. Initial investigations into this method found very poor agreement with mode impedances calculated by other workers [60, 61]. Other approaches were then looked at for more accurate results.

Finite difference methods are the least analytical and require large amounts of computing power and time [62]. The finite difference method is one of the oldest numerical methods for solving differential equations, one of the simplest applications is the solution of the two dimensional Laplace equation, from the solution of which, the inter-electrode capacitances of microstrip coupled lines can be found. The two dimensional Laplace equation is shown here

$$\frac{d^2v}{dx^2} + \frac{d^2v}{dy^2} = 0 \tag{2.43}$$

In order to obtain boundary conditions required to solve the problem the microstrip structure is placed in a metallic "box". To apply the finite difference technique the region defined by the box is discretized into a number of small, square regions, the corners of which define the

mesh or node points. The voltage at any node point can then be defined in terms of the voltage at an adjacent point using a Taylor expansion[56]. A typical grid point, not near any metallic boundaries, will have four adjacent points, if the Taylor expansion for each of these points is summed, it can be shown that [56, 57] that the voltage at the central points is the average of the four surrounding points i.e. if o is the central point, and a, b, c and d are the surrounding points we have

$$v_a + v_b + v_c + v_d = 4v_o \tag{2.44}$$

From a knowledge of the boundary conditions, the voltage at all node points can be found, from this the capacitance can be determined. The Taylor series used are truncated after terms in h^2, where h is the grid spacing, terms in h^4 are assumed to be very small, thus the grid size must be chosen such that this is the case.

A more numerically efficient technique is that of the spectral domain method [58, 63]. Initially this was a quasi-TEM technique but has been extended to account for the non-TEM dispersive nature of microstrip [40]. Here, the quasi-TEM technique will be discussed. The method uses a variational technique, this requires an expression which is at a stationary value when the desired function, in this case the scalar potential is a solution to the problem, i.e. a solution to Laplace's or Poisson's equations. Because the expression is at a stationary point, often a minimum, a series of trial functions for the unknown function can be tried until convergence at the minimum is obtained. In the spectral domain method the variational expression is arranged in terms of the inverse of the transmission line capacitance, in this case when the expression is at a minimum, a lower bound on the line capacitance is found, this in turn gives and upper bound to line impedance. The main feature of this method is that Fourier transforms are used to simplify Poisson's equation from a partial differential equation in the spatial domain, to an ordinary differential equation in the spectral or Fourier domain. A variational expression in the spectral domain is then obtained, trial functions are obtained for the charge distribution on the strip and a lower bound on the capacitance is

found.

Of these two latter methods the finite difference technique was investigated initially since it was felt that this approach, being more general would allow different conductor geometries to be analysed more easily, for example finite thickness conductors and more realistic conductor geometries such as trapezoidal conductors, caused by the etching techniques used to define the FET electrodes. It was also felt that it would be more straightforward to extend finite difference techniques from one to three coupled lines and moreover, a method that reduced the amount of computation time for the finite difference technique was obtained [50] and had been used successfully by other workers for two and three coupled lines [64, 65, 59].

2.3.2 The Resistive Network Analogue Technique

Introduction

The finite difference approach used is known as the resistive network analogue (RNA) technique [50, 51], although not widely used, this technique has shown to be reasonably accurate and computationally efficient by those who have employed it [50, 59, 64, 65, 66, 67, 68].

It was well known at the beginning of the twentieth century that the potential distribution around a set of metallic conductors could be found using the electrolytic tank method [69]. This method uses the fact that if the dielectric surrounding the conductors is given a small conductivity, then the current distribution that exists between the conductors is exactly analogous to the electric field for the lossless dielectric case [70]. These ideas led other workers, notably Kron [71], to look at the solution of more general differential equations by means of equivalent electrical circuits. One of the simplest examples of this technique is the representation of a transmission line as a set of series inductances and parallel capacitances, this equivalent circuit is the network analogue of the one-dimensional wave equation on a lossless transmission line. While Kron showed how these problems could be solved numerically, other workers e.g. DePackh [72] constructed physical networks of resistors and found the

potential distribution by measurement. Later Liebmann [51] described the RNA technique in more detail and re-examined the accuracies obtainable by the experimental methods and showed that accuracies of 0.1% to 0.01% were achievable with 1% toleranced resistors. Kron had shown how equivalent circuits could be used to solve very complex differential equations. In electromagnetics two of the common equations required to be solved are Laplace's and Poisson's equations, these are relatively simple differential equations, and using Kron's methods the only drawback was the amount of computer time required to solve them. This was a similar disadvantage to all finite difference methods, however, with the advent of large computing power these methods became more popular, which lead Lennartsson to look again at the RNA technique many years later [50]. Lennartsson proposed a method whereby the matrices that need to be inverted in order to solve the problem were reduced by one to two orders of magnitude whilst still retaining accuracies of better than 2%, dramatically reducing the amount of computing time required. In the following section Lennartsson's technique is outlined and extensions by other workers [64, 67] to open structures and finite thickness lines are also presented.

Lennartsson's Method

It has been discussed earlier how Laplace's equation can be represented by equation 2.44, figure 2.3 shows the local finite difference mesh for this equation

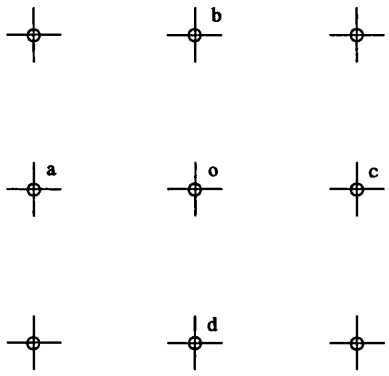

Figure 2.3: The nodes of the five point discrete Laplacian

In order to calculate the transmission line capacitance, the charge on the conductor must be found, thus Poisson's equation relating potential distribution and charge density is used, it is easily shown [57] that the finite difference form of Poisson's equation is

$$\frac{\epsilon_r(v_a - v_o)}{h^2} + \frac{\epsilon_r(v_b - v_o)}{h^2} + \frac{\epsilon_r(v_c - v_o)}{h^2} + \frac{\epsilon_r(v_d - v_o)}{h^2} = \frac{\rho}{\epsilon_o} \tag{2.45}$$

If resistors are introduced into the finite difference mesh as in figure 2.4 and Kirchoff's laws are applied to the central node, an expression for the current flowing into the central node can be written as in equation 2.46

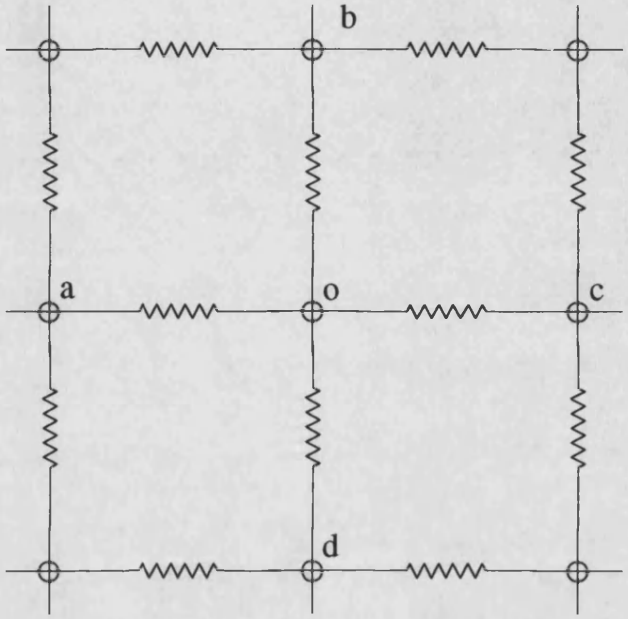

Figure 2.4: The resistive network analogue for the five point discrete Laplacian

$$\frac{v_a - v_o}{r} + \frac{v_b - v_o}{r} + \frac{v_c - v_o}{r} + \frac{v_d - v_o}{r} = I \tag{2.46}$$

If r is chosen such that $r = r_o h^2$ where r_o is an arbritary constant, it is seen that equation 2.46 is an exact analogue of equation 2.45. In the case of microstrip the value of ϵ_r is different above and below the strip, examining the above equations it is seen that if $r = \frac{1}{\epsilon_r}$ above and below the strip and $r = \frac{1}{\epsilon_r + 1}$ at the air dielectric interface, then the analogue is valid for the whole region. Comparing equations 2.45 and 2.46 it is seen that the current I flowing into the central node is proportional to the charge density at that node, thus if the currents flowing into all nodes occurring on the strip are summed then the total charge on the strip is found.

In order to find these currents, Lennartsson applies a recurrence relation to the resistive mesh and since all the resistors in the upper and lower regions are equal, expressions for a resistance matrix relating voltages and currents at the dielectric interface can be obtained. In order to speed up this procedure the recurrence relation is diagonalized, so that the inversions required are merely the inversion of the diagonal elements of a matrix. If the conducting strips are then introduced at the dielectric interface, the resistance matrix will be unaffected. Voltages are then imposed on all the nodes occurring on the strip, since no net current will flow from any other nodes and only the potential on the strips are of interest, the size of this matrix can be dramatically reduced. This reduced matrix can then be inverted to give the conductance matrix, and since the voltage for all nodes on one strip is equal, the sum of the node currents is found immediately, equation 2.45 shows that to obtain the capacitance, this sum is multiplied by ϵ_o, the free space permittivity. The self and inter-electrode capacitances are obtained directly by this method.

Discussion

There are a number of points worth noting about the method. In common with other finite difference methods a key point is the choice of mesh size. The mesh size must be small enough such that the initial Taylor series truncation is reasonably accurate, however, not so small that the computation time is too large. A typical mesh size used in this work is 0.5μm, this allows three nodes to be specified across a 1.0μm gate length, if smaller mesh sizes are used then the number of nodes on the much longer source and drain contacts makes the computation time too long. Ideally a finer mesh would be required in the gate region, with a coarser mesh for the rest of the structure, however this approach is not readily compatible with Lennartsson's method. Excellent agreement with other workers for mode impedances of two and three coupled microstrip lines are shown in chapter 4. For the wide FET structure, however, explicit values for inter-electrode capacitances are not normally found in the literature, estimates are normally made using closed form expressions [38] which suffer from the problems discussed earlier in the chapter. Thus, since reasonable accuracy had been obtained for "normal" microstrip structures it was felt that the technique could be

used for the wide FET structure as a good initial estimate of the capacitances, if this proved inadequate, further work would be undertaken.

With this order of mesh size, the computation time was typically 300-400 cpu minutes on a Hewlett Packard series 9000 mini-computer, used on a multi-tasked basis with approximately 2Mflops per user. This would normally allow two to three structures to be evaluated per day. This enabled a library of structures to be built up, the capacitances of which were stored in a look-up table for use in modelling and optimization procedures discussed in chapter 4.

Once the mesh size is specified, the external "box" that encloses the structure must also be specified. Typical box sizes for this work are 5000 x 5000, with 0.5μm meshsize this is equivalent to a 2.5mm x 2.5mm region. Care must be taken to ensure that the enclosure does not greatly effect the capacitances of the structure, but since the typical wide FET has a cross-section of less than 200μm and the GaAs substrate is 200μm high, this was found to be reasonable. To ensure minimal enclosure effect a number of workers [64, 67] have found asymptotic expressions for Lennartsson's recurrence relation such that the "top" of the enclosure can be removed to infinity, this procedure in fact reduces computation time since the whole of the upper region resistive network is modelled by a single expression.

In order to improve the calculated inter-electrode capacitances for the wide FET, finite thickness lines were introduced. Figure 2.5 shows a schematic of the FET structure around the gate, the three metal layers used in the fabrication process and discussed in section 1.3 are shown as M1, M2 and M3. This diagram is approximately to scale thus it is seen that the line thicknesses, even though in the order of a few microns, are not negligible relative to the line spacing between conductors.

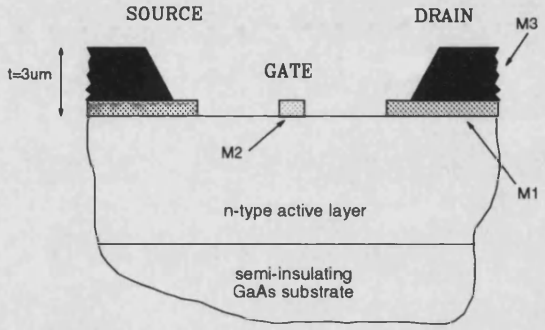

Figure 2.5: Detailed structure of electrodes of a wide FET

Although it is quite possible to analyse the structure as seen in figure 2.5 as a first approximation rectangular source and drain lines and a zero thickness gate line were assumed. The procedure for thick strips is outlined in by Tripathi [64]. The main requirement for thick strips and also strips at different levels is to define the resistance in Lennartsson's diagonalized form between nodes on different levels, in the same vertical column. Lennartsson's method can then be applied to find the node currents for all the nodes occurring on the strips. Since the charge will only be distributed on the surface of the conductor, the nodes within the strip will have zero net current flow, however, the resistance matrix for all the layers on the strip is still required to be inverted, thus the computation time for thick strips is somewhat increased. Up to five layers of nodes were used to define the strip thickness, thus for a 3μm thick strip the node spacing is fixed at 0.75μm. This therefore limits the number of nodes that can be placed across the strips and ultimately limits the accuracy achievable. It is possible to define different node spacings in the vertical and horizontal directions [64] and this could be the subject of future work. Results for finite thickness lines will be discussed in chapter 5.

2.3.3 Conclusions

A method has been presented for the calculation of inter-electrode capacitances for three coupled microstrip lines, from these the distributed admittance and impedance matrices are obtained. Other methods have been discussed and reasons for the choice of method have been given. Particular points of interest with regard to wide FET structures have been discussed. The wide FET electrodes have now be characterized, the next section will incorporate the intrinsic FET elements into the model, to obtain the complete immittance matrices for the structure.

2.4 Distributed Equivalent Circuit Model of a Wide FET

2.4.1 Introduction

In this section an equivalent circuit model will be obtained for the wide FET, from this the admittance matrix of the intrinsic FET is obtained, which when combined with the admittance and impedance matrices for the FET electrodes allows the complete S-parameters of the structure to be found.

Many workers have investigated the characteristics of wide FET structures [28, 32, 33, 34, 39, 42] these analyses have looked at the FET configured as a common source amplifier, in this work, for the first time to the authors knowledge, the wide FET is analysed in the unbiased "switching" configuration. As in the other quasi-TEM analyses discussed at the beginning of the chapter an equivalent circuit is required to model the intrinsic FET behaviour, the standard FET model developed in the early 1970's [73] is modified to account for the unbiased channel. The basic model is based on that discussed by Ayasli [74] and has been extended and given a more rigorous physical basis after Ladbrooke [38].

When constructing an equivalent circuit model each of the physical processes e.g. charge storage or resistive loss, occurring in the FET structure is modelled by a lumped element. Since the cross-sectional dimensions of the device are much smaller than the propagating wavelength, propagation effects across the device can be ignored, in a similar manner to the quasi-TEM approximation discussed earlier. This approximation has been found to give good results up to 20GHz [75]. Since the model is based on physical processes, ideally the parameters of the model should have a physical and geometrical basis. This has been achieved by Ladbrooke [38], however, this approach needs detailed knowledge of the device fabrication process, e.g. doping levels, gate length, implantation depth. If a standard foundry process is being used, the worker has no control over these parameters and the main use of this technique is in yield predictions and design centering. Since this work uses a standard foundry process, the only controllable parameters are FET source and drain electrode dimensions and

overall device width, thus provided the model can predict the effect of differences in these dimensions, there is no requirement in this work for a completely physical model.

The scheme adopted in this work is to obtain a lumped element model with a sound physical basis, then obtain estimates for the parameter values using physics based or empirical expressions combined with low frequency and d.c. measurements. S-parameters for the wide FET structure are obtained as outlined in the previous sections and compared with measured data from an initial device design. The elements of the model are then varied to obtain best fit to the measured data at a number of different bias levels. Initially this will be "manual" optimization where the parameters are adjusted individually, this is virtually a real-time process, since once the inter-electrode capacitances are found, the effect of changes in the circuit model are evaluated in less than 10 cpu secs on a series 9000 hp minicomputer. This optimization procedure could be speeded up by use of optimization algorithms which perform multidimensional data fitting, however only manual procedures are used in this work, other numerical procedures could be the subject of future work. Once a good fit is obtained the model can then be used to investigate different device applications which will be discussed in chapter 6.

As in the other analyses of wide FETs [28, 32, 33, 34, 39, 42] the models discussed in this chapter are based on an infinitely short section of the device and all elements are "per unit length". This implies uniformity in the propagation direction, this will be discussed in chapter 4 when the device structures will be shown in detail. The models developed here are small signal, that is they are linear with respect to power level, for the applications investigated in this work a small signal model is adequate.

2.4.2 Basic Model

In order to construct the equivalent circuit a knowledge of the FET structure is required, a schematic of a typical FET is shown in figure 2.6

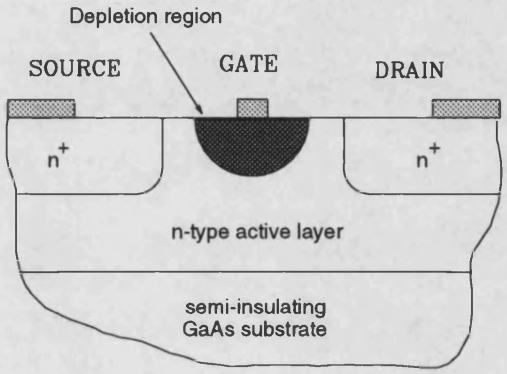

Figure 2.6: FET structure

The main features of the FET structure are the active layer which forms the channel region, the depletion region formed beneath the gate line Schottky-barrier contact, and the source and drain ohmic contacts providing connections to the channel region. In the switching configuration, there is no source-drain bias current, thus the depletion region is symmetric about the gate line. The FET electrodes are assumed to be symmetrical about the gate line, for the foundry process used in this work, this has found to be the case. Any slight asymmetries will be averaged to maintain symmetry. The basic equivalent circuit associated with this structure is shown in figure 2.7

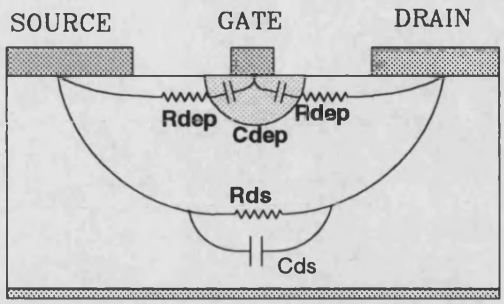

Figure 2.7: Basic FET model

The elements in the circuit are :

(i) Channel resistance, R_{ds}, this is the ohmic resistance of the n-type active layer.

(ii) Drain-source capacitance, C_{ds}, capacitance between the drain-source electrodes.

(iii) Depletion capacitance, C_{dep}, capacitance associated with the charge storage in the depletion region.

(iv) Depletion resistance, R_{dep}, ohmic resistance associated with the non-ideal depletion capacitance.

Of these elements it was felt, initially that C_{ds} was adequately modelled within the static inter-electrode capacitances calculated previously by the RNA technique and the ohmic contact resistances were included in the channel resistance.

The modelling scheme discussed earlier, requires the modelled S-parameters to be fitted at a number of gate bias points, these points were chosen as : zero bias, pinch off and a mid-bias point. Thus, for the bias dependent parameters, three values are required corresponding to each of the bias points, allowing the model to be evaluated separately at each bias point.

Initially R_{dep} was set constant with bias, thus there are two bias dependent parameters, C_{dep} and R_{ds}. R_{ds} was set using d.c. resistance measurements and low frequency S-parameter measurements, the method for this will be discussed in chapter 4. Ayasli [74] gives an empirical expression for the pinched off depletion capacitance as

$$C_{dep} = 60\frac{l_g}{a} \tag{2.47}$$

Where C_{dep} is in picofarads per unit of gate width, l_g is the gate length in microns and a is the depth in microns of the active layer beneath the gate. The mid-bias point and zero bias capacitances were set as multiples of this capacitance, since at pinch off the depletion capacitance is at a minimum. Since these capacitances were to be optimized, accurate expressions for these initial estimates were not required.

The elements of the model have been defined at the three bias points, the three-port admittance matrix for the circuit model is now required to combine with the FET electrode admittance matrix. If the series R-C combination associated with the depletion region is converted to parallel form as shown here

$$\begin{aligned} Y_{dep} &= \frac{(\omega C_{dep})^2 R_{dep} + j\omega C_{dep}}{1+(\omega C_{dep} R_{dep})^2} \\ Y_{dep} &= G_p + j\omega C_p \end{aligned} \tag{2.48}$$

The admittance parameters or Y-parameters for the model are then

$$\begin{aligned} Y_{11} &= G_p + G_{ds} + j\omega C_p \\ Y_{22} &= 2G_p + 2j\omega C_p \\ Y_{12} &= -G_p - j\omega C_p \\ Y_{31} &= -G_{ds} \end{aligned} \tag{2.49}$$

Note that Y_{21} and Y_{31} are negative due to the definition of Y-parameters.

The total admittance matrix, Y_T, is then the sum of that defined in equation 2.49 and the inter-electrode admittance matrix. All the normal mode parameters of the structure can then be evaluated as shown earlier, note that Y_T is frequency dependent, thus it must be evaluated at each frequency point, giving frequency dependent normal mode parameters.

The intrinsic FET admittance matrix is seen to contain conductance elements, this is therefore no longer a lossless system. The theory developed in section 2.2 is completely general and allows for both parallel conductance and series resistance. The addition of parallel conductance is analogous to embedding the transmission lines in a lossy dielectric medium, this does not affect the Quasi-TEM approximations required for this analysis since it can be modelled by replacing the dielectric constant, ϵ, with a complex dielectric constant, which does not alter the solutions to Maxwell's equations [63].

This basic model was used for initial modelling, results for the model are shown in chapter 4. Although reasonable results were obtained, a number of improvements to the model were made to give a more detailed representation of the physical structure, these are discussed in the next section.

2.4.3 Improved Model

The basic model had achieved reasonable results and many of the trends observed in the measured results were well reproduced. It was felt that this simple model could be enhanced to give improved model performance.

One of the first improvements required was highlighted when improved test fixtures allowed full six-port characterization of the device. This enabled the gate associated S-parameters to be measured, these showed that the gate line has very high d.c. resistance, this was confirmed by simple d.c. measurements. The electrode resistances were found to be of the order

of 100Ω to 200Ω for a 1.5mm device. It was obvious such a large effect had to be included in the model. Unlike the inclusion of parallel conductance discussed above, the inclusion of series resistance in the model implies an E-field in the direction of propagation, thus invalidating the quasi-TEM approximation. In order to maintain the quasi-TEM approximation the magnitude of this longitudinal component must be assumed small compared with the transverse component, this was assumed to be the case, as in other work [34]. The d.c. resistance and the lossless inductance of the line can be modified, assuming a small magnitude of longitudinal electric field, by introducing the idea of internal distributed impedance [70]. This is in fact a way of modelling the skin effect mentioned earlier. Expressions for these internal impedances can be obtained by modelling the situation as a plane wave incident on and perpendicular to the conductor. The internal impedances are complex, the real part gives the internal resistance and the imaginary part can be expressed as an inductance, both of these quantities are found to be frequency dependent. Earlier it was stated that the skin depth for gold at 10GHz was 0.79μm, thus since the dimensions of the gate are smaller than this, its resistance can be represented by the d.c. value. Initially the series resistances of the source and drain lines were also represented by their d.c. values, and the inductance was unmodified, the results obtained were reasonably good, as a further extension the internal impedance components could be included.

The resistive effect of the n^+ regions beneath the source and drain lines was then included in the model. This introduces much greater complexity into the Y-parameters of the model, but using the symmetry of the structure relatively simple expressions are obtained.

An effect that had not been taken into account is that caused by the gate depletion region on the inter-electrode capacitances [38]. An electric field exists within the depletion region due to the fixed charge contained within it, this electric field "masks" the inter-electrode fields to the under side of the gate. Thus only the capacitances on the "air" side of the gate are included in the model. In order to calculate the "air-side" capacitances for the gate, the fact that two sets of capacitances are calculated is used. The first set is with no dielectric, used to calculate the inductance matrix, as discussed in section 2.3 and the second is with dielectric

to give the actual inter-electrode capacitances. Considering the non-dielectric capacitances, the gate to drain (C^a_{21}) and gate to source (C^a_{23}) capacitances (symmetry implies $C^a_{21} = C^a_{23}$) can be thought as having two components, an upper and lower component, assuming these to be equal then the required "air side" capacitance is simply half of C^a_{21}. This assumption implies that the ground plane has a small effect on these capacitances, this has been checked as being valid by placing the ground plane at infinity by using the asymptotic expressions discussed in section 2.3 and obtaining differences in C^a_{21} of less than 0.75%. Since the under side of the gate is masked, the capacitance of the gate line to ground must also be set to zero.

A further modification to the model was sought after the model had failed to predict an optimum electrode geometry for a particular application to be discussed in detail in chapter 4. Even though the model predicted the performance of the initial test structure well, the measured data for the third iteration device differed greatly from the model's prediction. It was found that by increasing the drain - source capacitance, the fit of the data improved dramatically. This led to a re-investigation of the nature of the C_{ds} component. Careful reading of Ladbrooke's text [38] highlights the fact that there is another component to C_{ds}, over and above the inter-electrode component, associated with the proximity of the n^+ regions either side of the gate line, seen in figure 2.6. Field lines will pass between the two n^+ regions creating a capacitive effect. The magnitude of the capacitance was found by fitting to S-parameter data as before, the fit obtained with the inclusion of this capacitance was very good for all devices modelled.

The final model is shown in figure 2.8 with the inter-electrode capacitances and inductances omitted to aid clarity.

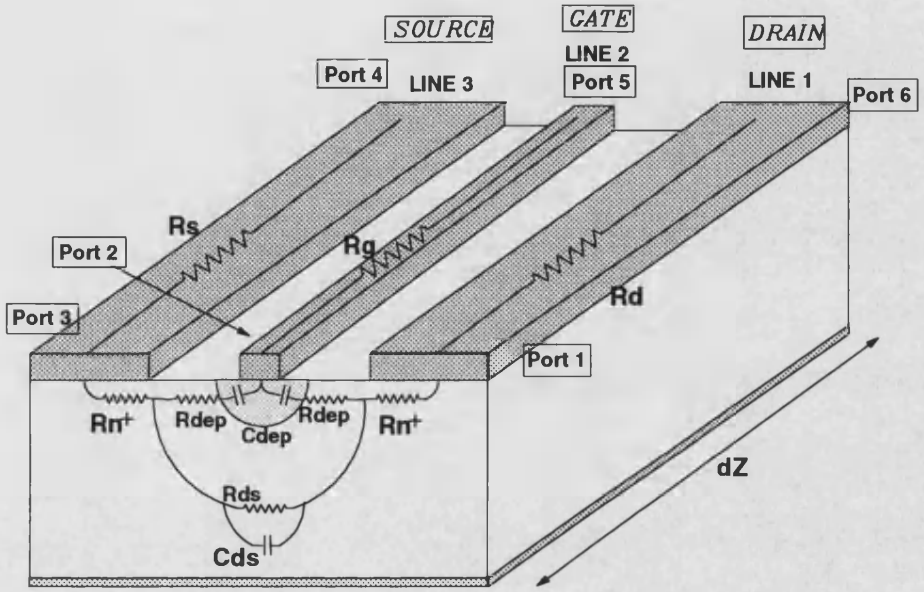

Figure 2.8: Final wide FET model

The parallel admittance and series impedance matrices are now required to calculate the full six-port S-parameters of the wide FET structure. In order to calculate parallel admittance parameters (Y-parameters) a short circuit current is imposed upon one port and the voltage measured at the port of interest, with all other ports short circuited. Thus for Y_{31} a short circuit current is imposed at port 3 and voltage is measured at port 1 with port 2 short circuited, in figure 2.8 this results in a chain of components between ports 1 and 3, this is solved using ABCD parameters. For Y_{21}, it is seen the calculation is complicated by the presence of R_{n+}, with current injected at port 2 and port 3 shorted, Y_{21} becomes dependent on the channel parameters C_{ds} and R_{ds}. However, if R_{n+} is assumed equal at ports 1 and 3 then the potential at either end of the channel parameters will be equal and thus they will have no effect. This has been checked as being valid using a commercial circuit simulator. The Y-parameters for the intrinsic FET are then added to the Y-parameters for the electrodes to give the total parallel admittance matrix for the structure. The total series impedance matrix is found by adding the electrode resistances to the inductance matrix of

the electrodes. The full six-port S-parameters for the structure can now be found.

2.4.4 Conclusions

An initially simple model has been improved to reflect the physical structure beneath the gate more rigorously, this has been used to obtain very good S-parameter fits for a number of device structures, these results will be shown in chapter 5. The model can now be used to understand and improve the performance of many devices based on wide FET structures, some of which will be discussed in later chapters.

2.5 Inclusion of Parasitics

2.5.1 Introduction

A model for the complete structure has now been obtained, in order to obtain measured data for fitting of the model, the devices must be connected to measurement instrumentation, in so doing extra parasitic effects are introduced which can greatly mask the intrinsic device performance. The final test set up used in this work is shown in figure 2.9

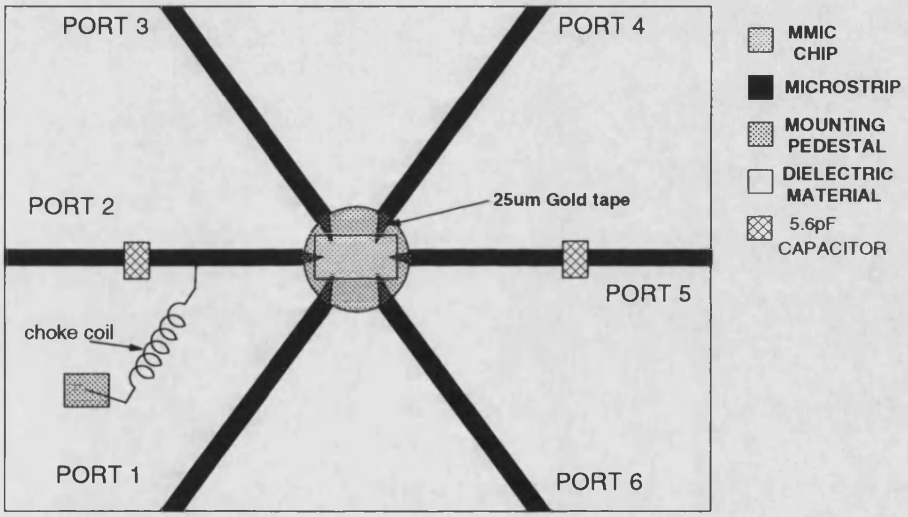

Figure 2.9: MMIC mounting fixture

The MMIC is soldered to the central brass pedestal, the six ports of the wide FET are connected to incoming microstrip transmission lines by either wire or tape bonds. The inductance of these connections is the major parasitic. The microstrip lines also add phase shift, small insertion loss and reflections from input and output. Figure 2.9 also shows the d.c. blocking capacitors and choke coil for biasing the gate line, these too add to the circuit parasitics.

There are two approaches to the problem of parasitics, either the intrinsic device data can be "de-embedded" from the measured data using models for the parasitics or, if a device model

is available, it can be embedded in the parasitics. The choice of approach depends upon the application, if the intrinsic device data is required and there is no adequate device model, then the former approach is preferred. However, with multiport devices such as directional couplers and mixers, the de-embedding techniques required become quite complex [76]. In this work, since a device model is available, the embedding approach is taken. There are various techniques to embed devices in parasitics, they will be outlined and discussed in the next section.

2.5.2 Methods of Including Parasitics

Three methods have been investigated in this work :

(a) Mason's non-touching loop rule

This method was developed by Mason [77] and uses the flow graph technique to describe a network. The flow graph is a visual illustration of how power flows through the network. Each port of the network has two nodes, an input and an output node, these represent the power wave variables which define S-parameters discussed in section 2.2. All the nodes of the network are connected by branches, each branch has a value which defines the direction of power flow and the relationship between the power waves entering and leaving the branch, i.e. an S-parameter. The power wave leaving a node can be shown to be equal to the sum of the branches entering the node. This is a very powerful technique and allows many problems in microwave engineering to be solved by inspection together with very basic algebra.

For complex networks, purely algebraic methods can become cumbersome, to aid the analysis, Mason developed a method [77], that can solve networks purely by applying a simple rule, no matter what the complexity. In practice this method of manual solution is limited to networks with four or less ports. A method has been developed by Somlo [78] which allows more complex networks to be solved and results in algebraic expressions relating input and output power waves. The basis of Mason's rule is to find the path or paths which connect

the nodes of interest, then find all the closed loops in the network and note those that do not touch the path of interest. Somlo's method uses a computer algorithm to automate this searching process.

This method was applied initially to a four-port network, which represented the wide FET with an open circuited gate line. Two-port networks were then added to each of the four ports of the FET structure, representing the parasitic elements, and algebraic expressions were obtained for the total S-parameters. The expressions were very lengthy, however, once entered into the model correctly, gave accurate results when compared with the circuit simulator method. However, for the full six-port, it was felt, even this improved method was impractical.

(b) Commercial Circuit Simulators

In this method the device S-parameters are imported into a commercial simulator, any number of parasitics can then be added and the full S-parameters obtained. There are a number of problems associated with this method :

- If the system used for calculation of the device S-parameters is networked to the circuit simulator, this method is usable, if not, it becomes impractical.
- The devices modelled in this work are mostly six-ports, some simulators are not able to import S-parameter data for devices with more than four ports, this limited the choice of simulator.
- In this work, three bias levels are being modelled, this requires three different sub-circuits to be used, which greatly increases the simulation time.

The main problem, however, with this approach is that if any of the device model parameters are changed, the new device S-parameters must be imported for each iteration, this quickly becomes impractical. Simple device models can be incorporated into some circuit simulators,

to incorporate the models used in this work would require converting many hundreds of lines of computer code to that used by the circuit simulator, this was seen as impractical.

The one main advantage of this method is that built in optimizers in the simulator can be used to obtain the correct level of the circuit parasitics. This advantage is greatly out weighed by the other factors discussed above. Other methods which did not rely on simulators were sought.

(c) The Multiport Connection Method (MPCM)

This method was developed by Monaco and Tiberio [79] and allows for the arbitrary interconnection of multiport networks. From a knowledge of the S-parameters of the individual networks, the overall S-parameters for the network can be derived.

The system of networks of interest in this work is shown in figure 2.10

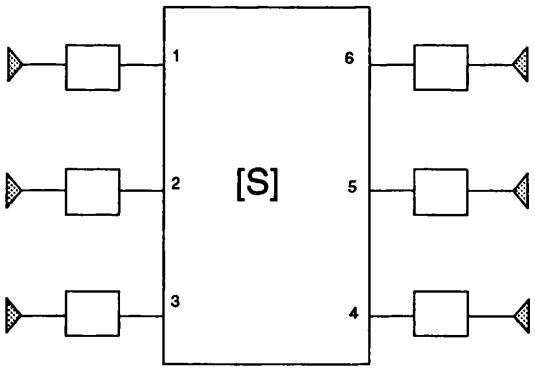

Figure 2.10: The multiport connection method

The central six-port represents the wide FET device, the six two-ports networks are the parasitic connections to the device, which could be simply inductances, or more complex two-ports formed by the combination of inductances and transmission lines. All the ports of the structure are numbered and the wave variables (power waves) associated with each port are divided into internal and external types. There will only be six pairs of external wave variables, those at the output of the parasitic elements. The relationship between internal and external wave variables can be written in matrix form

$$\begin{bmatrix} b_p \\ b_c \end{bmatrix} = \begin{bmatrix} S_{pp} & S_{pc} \\ S_{cp} & S_{cc} \end{bmatrix} \begin{bmatrix} a_p \\ a_c \end{bmatrix} \tag{2.50}$$

Where p denotes the external ports and c denotes the internal ports, S_{pp} are the input S-parameters of the external ports, S_{cc} are the six-port S-parameters, and S_{pc} and S_{cp} are the transmission S-parameters which relate internal and external wave variables. A connection matrix Γ is then defined which describes the interconnection of the internal ports

$$b_c = \Gamma a_c \tag{2.51}$$

The matrix Γ contains ones and zeros, a one denotes a connection and a zero no connection. Combining equations 2.50 and 2.51

$$\Gamma a_c = S_{cp} a_p + S_{cc} a_c \tag{2.52}$$

Rearranging

$$a_c = (\Gamma - S_{cc})^{-1} S_{cp} a_p \tag{2.53}$$

Substituting this in 2.50

$$b_p = (S_{pp} + S_{pc}(\Gamma - S_{cc})^{-1} S_{cp}) a_p \tag{2.54}$$

Which gives the total network S-parameters, S_n as

$$S_n = S_{pp} + S_{pc}(\Gamma - S_{cc})^{-1}S_{cp} \tag{2.55}$$

This method has been implemented and gives identical results to those obtained from the circuit simulators. This approach allows all the parameters of the model, both parasitics and the intrinsic device, to be varied, and the results obtained very rapidly, typically less than 10 seconds on a HP series 9000 mini-computer. The approach is very flexible, once the required matrices are defined, very complex networks can be analysed, which could only be otherwise analysed using circuit simulators. Some of these complex networks will be discussed in chapter 6.

2.5.3 Conclusions

In this section the problem of parasitics caused by the mounting of MMIC devices as been addressed. A number of methods have been discussed, advantages and disadvantages of the methods have been outlined. Finally, a flexible and efficient method has been described, whereby using the MPCM the effect of circuit parasitics can be modelled for multiport devices. Results using this method will be shown in chapter 4 and applications of the method to more complex networks will be discussed in chapter 6.

2.6 Summary

In this chapter a symmetrical wide FET structure has been analysed. It is believed by the author that this is the first such analysis carried out on a wide FET structure configured in the switching configuration, with no drain-source bias and an ungrounded source. The analysis used has been compared with other methods and the reason for choice of methods given.

The analysis uses a coupled mode method [43, 44, 45] and all the propagation characteristics of the structure are defined in terms of the electrode distributed admittance and impedance matrices. A method for the calculation of the electrode admittance matrix has been introduced and compared with other possible methods. An equivalent circuit model for the intrinsic FET has been used to obtain the FET distributed admittance matrix. Improvements to the model have been introduced to give it a more rigorous physical basis. Finally, the parasitics introduced by the measurement fixture have been included in the model and a number of possible techniques have been discussed in detail. The method chosen allows fast and accurate analysis of the whole model, parasitics and intrinsic device, simultaneously.

The model developed will be compared with measured data for a number of different structures and the element values obtained by fitting to the measured data. The model will then be used to predict the performance of the device in a number of applications which will be discussed in chapters 4, 5 and 6.

Chapter 3

Measurement Techniques

3.1 Introduction

Much of this work is concerned with the measurement of microwave devices, these measurements are used to validate models for devices, which are then used predict their performance under different measurement conditions or with different geometric structures. It is important that the effects of the measurement test fixtures into which the devices are mounted are included in the model or are reduced to an insignificant level. In chapters 4 and 5 it is seen how the test fixture can greatly affect the performance of a microwave device.

In this chapter a number of measurement related issues are discussed. Firstly, a detailed description of the microstrip mounting fixture used in this work is given. This is followed by a section discussing the particular problems associated with multiport device measurements. Many of the devices in this work require d.c. bias to be applied to their ports. The circuits used to apply the bias can greatly affect the performance of the device. This chapter discusses how these circuits can be designed to have minimum effect. The extra effects introduced by test fixtures are often termed "parasitics", if their effect is to be included in a circuit model, estimates of their level must be made. Results for the parasitics associated with the test fixtures used in this work are presented here. Finally some conclusions are drawn.

3.2 Mounting MMICs

MMICs are often an order of magnitude smaller than standard MIC hybrid circuits [38], thus they present particular measurement problems. The first problem encountered is that of connecting the ports of the MMIC, typically 120μm square bond pads, to the ports of the measurement apparatus, in this case 3.5mm coaxial connectors. The connections must have sufficiently good microwave performance such that they do not dominate the total measured response. The MMIC must also be mounted in such a way that repeatable measurements can be performed so that comparisons between devices can be made. In this work this is achieved using a hybrid MIC mounting circuit, in recent years on-wafer probing [80] has allowed almost direct connection to the MMIC bond pads, probing will be discussed in more detail in the next section. The mounting fixture and hybrid circuit is shown below

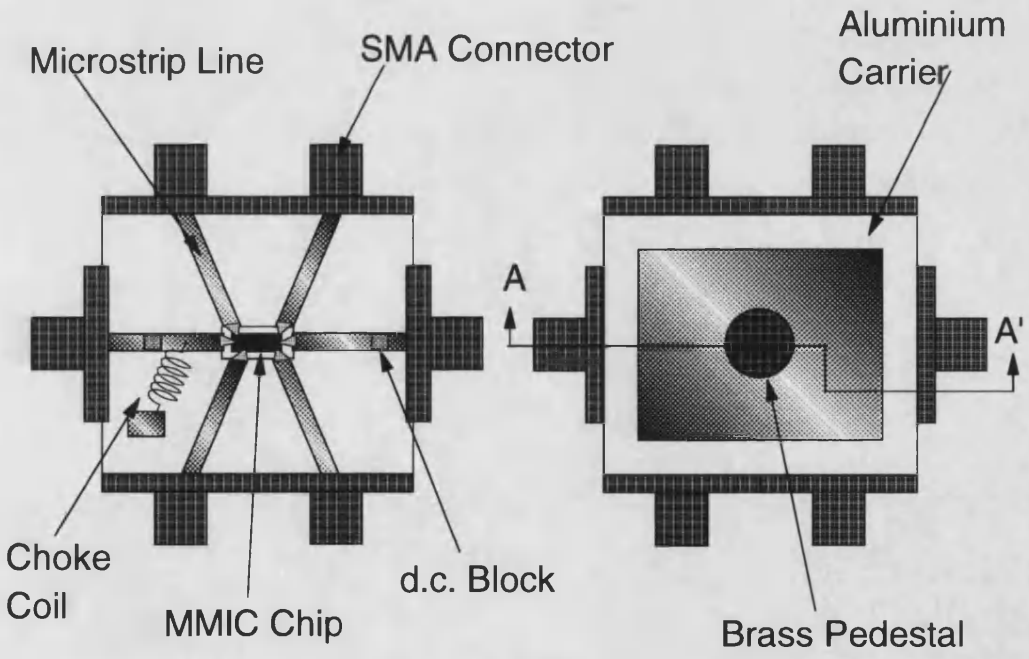

Figure 3.1: Topside and underside of MMIC test fixture

Figure 3.1 shows a 1 inch square RT-duroid^{TM} board with six 50Ω microstrip transmission lines. The MMIC is mounted centrally and soldered to a brass pedestal. The microstrip lines are tape bonded to the on-chip bond pads using 25μm thick gold tape. The microstrip circuit is supported by an aluminium carrier, which has had its inner section removed to prevent grounding and resonance problems caused when a large area is required to be grounded. A more detailed view of the fixture is shown in figure 3.2

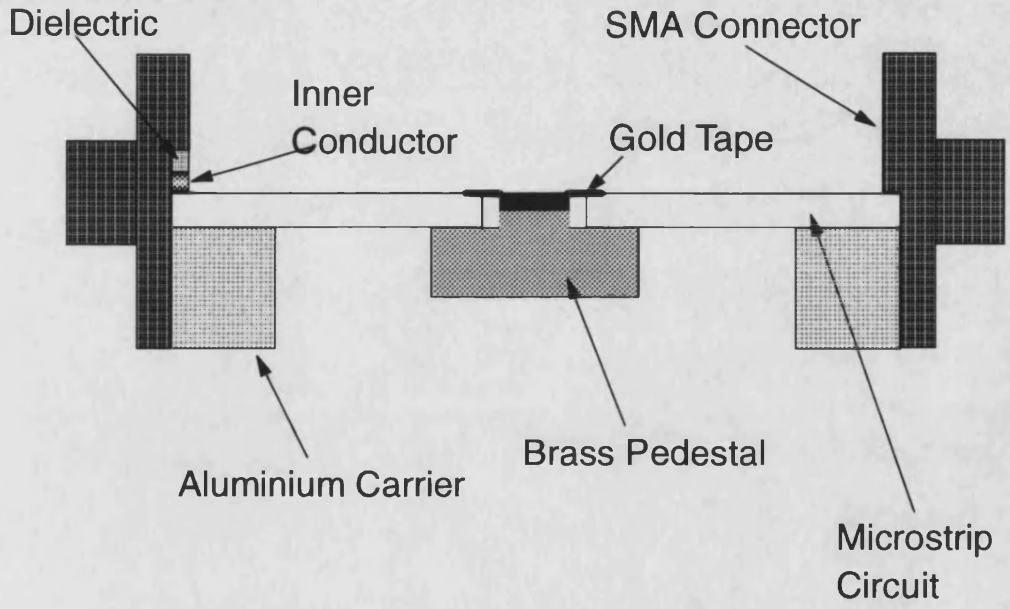

Figure 3.2: Cross-section A-A′ of MMIC test fixture

The figure shows that the brass pedestal has a rectangular section machined onto the top face onto which the MMIC chip is soldered. Prior to soldering the MMIC a rectangular section is cut in the microstrip circuit and the pedestal inserted and soldered to the ground plane metallization of the microstrip board, this ensures ground plane continuity from the MMIC to the microstrip circuit. Gold tape is then soldered from the microstrip line to the on-chip bond pads. To ensure low parasitics the length of the tape bond must be kept to a minimum. To achieve this the rectangular machined section on the brass pedestal and the rectangular aperture in the microstrip circuit must be as close to the size of the MMIC as possible.

The SMA connectors are compatible with the 3.5mm connectors of the measurement apparatus, in this case a HP8510B vector network analyser(VNA). The connectors are screwed to the aluminium carrier, the centre conductor of the connector connects to the microstrip line. In order to hold the microstrip circuit firmly in place, and more importantly to ensure ground plane continuity between the connector and the microstrip circuit, the connector has been modified to provide both of these functions. The lower half of the front face of the connector is machined back by $\simeq$1mm, without damaging the centre conductor. The figure above shows how this provides a surface which can exert downward force on the edge of the microstrip circuit ensuring good grounding of the circuit to the carrier. Care must be taken to ensure that the centre conductor can still contact the microstrip line.

This scheme has been used successfully in this work to characterize MMIC devices up to 20GHz. The fixture provides a low cost, low parasitic and repeatable mount for MMICs. The fact that soldering of the connectors to the microstrip lines or of the board ground plane to the carrier is not required means that boards can be reused many times before connections start to degrade. The fixture can be easily adjusted for different board thicknesses and circuits with areas as large as 6 square inches have been successfully measured using larger aluminium carriers.

3.3 Measurement of Four and Six Port Devices

3.3.1 S-parameter Measurements

The wide FET studied in this work is configured firstly as a four-port and later as a six-port. The measurements are carried out using an HP8510B vector network analyser. This instrument has two measurement ports, thus for devices with more than two ports the problem arises of how to terminate the unused ports which has implications for the accuracy of the S-parameter measurement. In recent years the problem of multiport S-parameter measurement has received much attention [81, 82]. The growth of the MMIC market has meant that accurate multiport characterization is required to be carried out on-wafer, and using a combination of wafer probers and broadband switches, accurate, on-wafer measurements of multiport devices have been achieved.

In this work, a probe station was not available, thus the device had to be measured using the fixtures discussed above. In order to measure the forward coupling of a wide FET, 50Ω terminations were placed on ports 2, 3, 5 and 6, when measuring the six-port S-parameters. In order to discuss the problems that arise from this situation, a simpler two coupled line circuit is used as an example. The circuit and its terminations are shown below

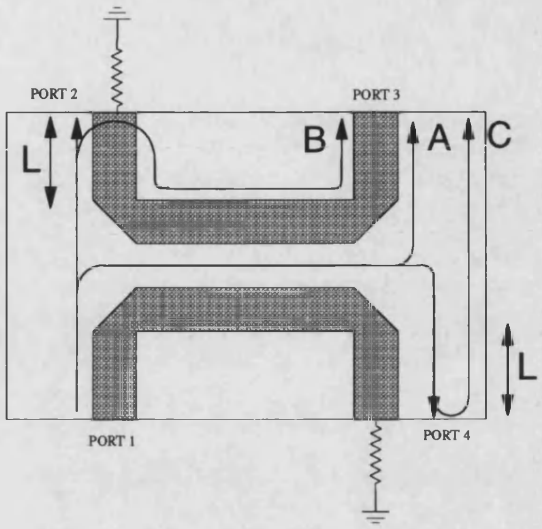

Figure 3.3: Two coupled lines showing forward coupling measurement

In the figure ports 2 and 3 are terminated in 50Ω loads, the arrowed lines show the important power flows through the circuit. Power is incident on port 1 and couples backwards to port 2, some fraction of this power will reflect from the termination of port 2 and pass to port 3, similarly power passing to port 4 will reflect and couple to port 3. Thus at port 3, there are three major signal components, A : the forward coupled signal, B and C : reflected signals. For this symmetrical situation, the B and C components will be in-phase, however, the forward coupled signal has a path length shorter by a distance L. This path length difference will produce an interference effect at port 3, where the signals will undergo phasor addition. This produces a rippling effect with frequency since the phase difference will depend upon the frequency. Using simple mathematical expressions information about the magnitude of the forward coupled and reflected signals and the length, L can be extracted from the measured forward coupling response.

Considering the interference of only two signals (since B and C are in-phase), the phase difference between signal A and B is 2βL, where β is the lossless propagation constant of the line length, L. When the phase difference is an even multiple of 2π radians the signals

will add in-phase producing a maximum. Thus a ripple pattern is produced as the signals add in and out of phase. The frequency difference between two maxima can be related to the difference in path length, L. An expression for the phase difference between two adjacent maxima at frequencies, f_1 and f_2 is given below

$$2\beta_1 L - 2\beta_2 L = 2\pi \tag{3.1}$$

Knowing that

$$\beta = \frac{2\pi f}{c} \tag{3.2}$$

Where c is the free space velocity of light and expression relating path length difference to ripple frequency can be written

$$L = \frac{c}{2\Delta f} \tag{3.3}$$

Remembering the speed of light is less in a dielectric medium a more general expression is

$$L = \frac{c}{2\Delta f \sqrt{\epsilon_{reff}}} \tag{3.4}$$

Where ϵ_{reff} is the effective dielectric constant of the medium. Expressing frequency in GHz and L in mm the expression can be further simplified

$$L(mm) = \frac{150}{\Delta f(GHz)\sqrt{\epsilon_{reff}}} \tag{3.5}$$

This expression is used to analyse the forward coupled response of the wide FET measurements in chapter 5. The rippling effect also means that the actual forward coupled signal will be less than the measured signal, by up to a maximum of 6dB if the two interfering signals are of equal amplitude.

3.3.2 On-Wafer Probing

The use of on-wafer probing has in recent years resulted in highly accurate characterization of two-port devices on-wafer [80, 83]. The combination of these techniques with automated multiport measurement techniques [82] which employ broadband switches and de-embedding techniques, results in the ability to characterize accurately multiport devices on-chip.

The devices fabricated as part of this work have all been designed to be compatible with on-wafer probing, since this technique would allow the intrinsic device performance to be measured. It is hoped that in future work probed measurements will be carried out and the performance of these devices, unaffected by mounting circuit parasitics will be obtained.

The fundamental element of an on-wafer probing system is the probe tip, this contacts the on-chip probe pads as shown below

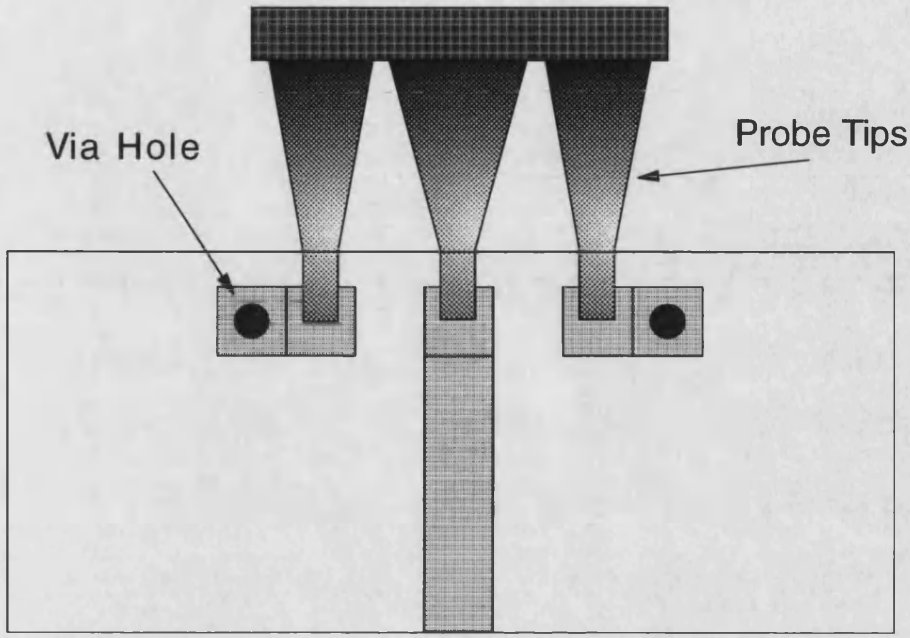

Figure 3.4: Wafer probe tip contacting on-wafer bond pads

The probe shown here is an air-coplanar probe [83], rather than the more usual coplanar-on-alumina probe, the air probe gives improved visibility on-chip, better insertion loss and better mechanical characteristics. The signal is applied to the central finger, the outer fingers give the probe a coplanar configuration allowing a constant 50Ω impedance level to be maintained along the length of the probe.

In order to calibrate the system, on-chip standards are used, a popular scheme is the TRL(Through-Reflect-Line) method [84], in which no high precision 50Ω loads are required and the measurements are referenced to an on-chip 50Ω transmission line.

Thus on-wafer probing would allow full characterization of the devices measured in this work, giving accurate and repeatable measurements well into the millimetric frequency range.

3.4 Active Device Bias Circuits

When measuring active devices d.c. bias must be applied to the device. In a microwave measurement system this is not a straightforward task, since the bias circuits can often greatly affect the performance of the device [53]. When measuring two-port circuits using the HP8510B VNA bias can be applied using the instruments' internal, high performance bias tees, however, for multiport applications this is not always possible. In this case bias circuits must be designed on the mounting substrate.

A simple bias circuit has two elements, one which prevents microwave signals from passing into the d.c. power supply or low frequency electronics and another which prevents the d.c. component from passing to other parts of the microwave circuit. The first of these functions is normally performed by an inductor and the second by a capacitor. These functions can also be realized using low pass or high pass filter networks, which can be implemented as lumped or distributed components.

In this work the r.f. blocking function was initially implemented using a high impedance transmission line. The results in section 4.3 show that there is a large resonance associated with this structure, the inductance of the line is resonating with the capacitance of the large bond pad on the microstrip board. The performance of the structure was measured separately, connected to a 50Ω transmission line, the results are shown below

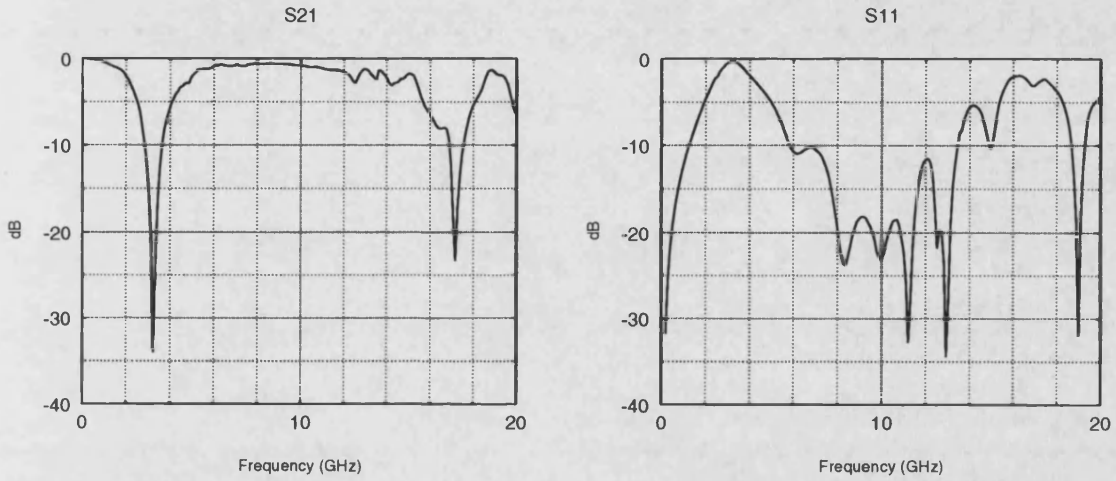

Figure 3.5: Transmission line choke in parallel with a 50Ω transmission line

The large resonance at 3GHz, dominated the low frequency performance of the device under test. Other methods of implementing the high pass function were sought. It was decided to using a lumped element approach and produce an inductor from a wire wound coil. This is a well used technique in hybrid circuit design and uses enamel coated wire wound on to a small diameter former. The performance of a coil is shown below for eight turns of 0.21mm diameter enamel wire wound on a 2.5mm former

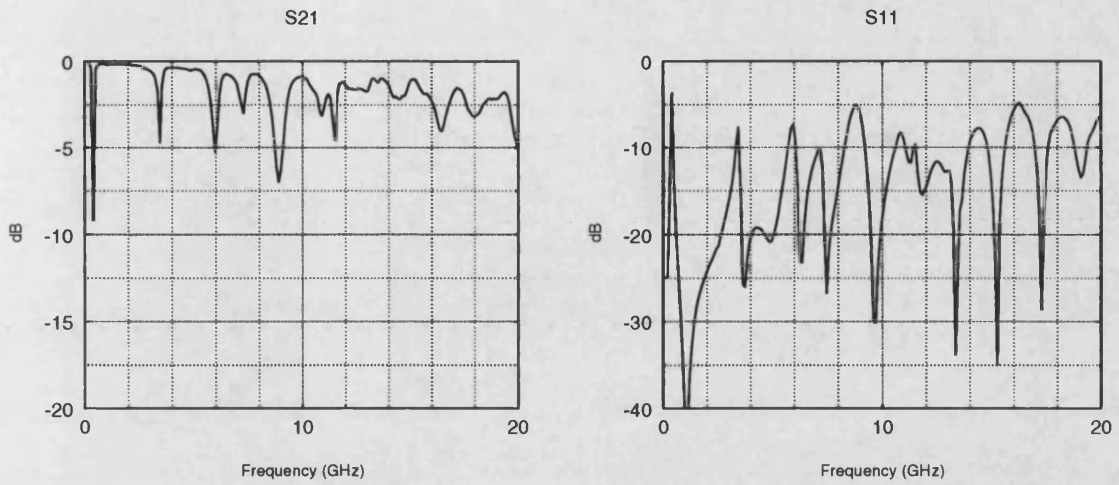

Figure 3.6: Wire wound coke coil in parallel with a 50Ω transmission line

While the frequency of the first resonant frequency is much reduced, as expected with the large increase in inductance, there are a large number of higher frequency resonances, producing poor performance across the whole band. These resonances are caused by interwinding resonances in the coil, and these can be damped by coating the coil in a lossy material [85]. The lossy material must be capable of being applied to the coil, a efficient method for this is to use carbon loaded epoxy. Carbon powder is added to an epoxy, then applied to the coil, the epoxy sets and the coil can be soldered into a circuit. The optimum performance was found with a 6mm long coil of 2mm diameter using 0.21mm diameter enamel wire, the performance is shown below

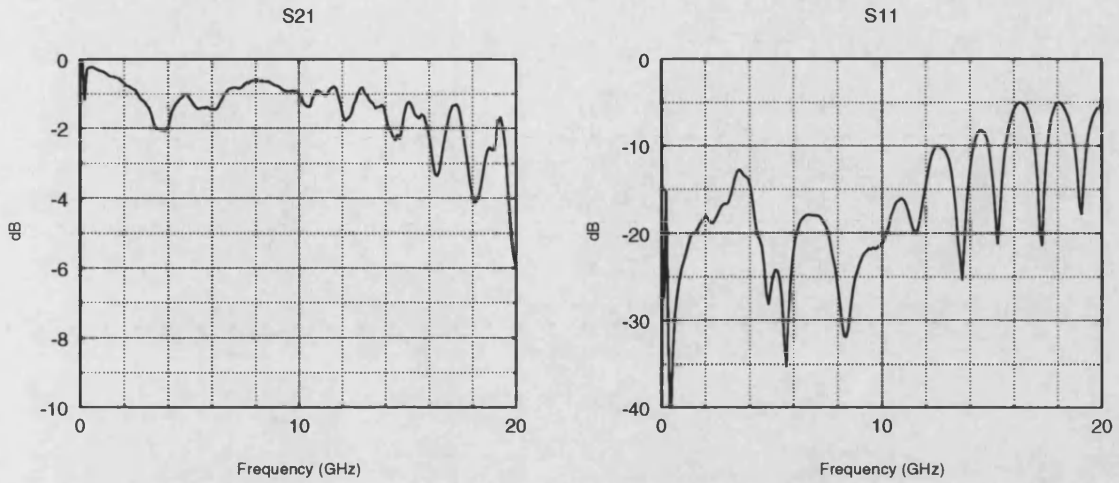

Figure 3.7: Wire wound coke coil coated with lossy epoxy in parallel with a 50Ω transmission line

These results show very good broadband choke performance with less than 2dB through transmission up to 10GHz, above 10GHz the results are dominated by the 50Ω line performance as will be seen later in the section. Thus a low cost, high performance choke coil has been implemented, which allows the characterization of active circuits from 0.1GHz to 20GHz.

The second part of the bias circuit is the d.c blocking element, initially, no d.c. blocks were used, and when 50Ω terminations were attached to the gate line, high currents flowed resulting in damage. It was thus important to implement the d.c. block. Multilayer chip capacitors were available but their microwave performance was found to be poor. Single layer ceramic capacitors give much better performance and a low value capacitor was obtained, C=5.6pF, this was measured in series on a 50Ω line, results shown below

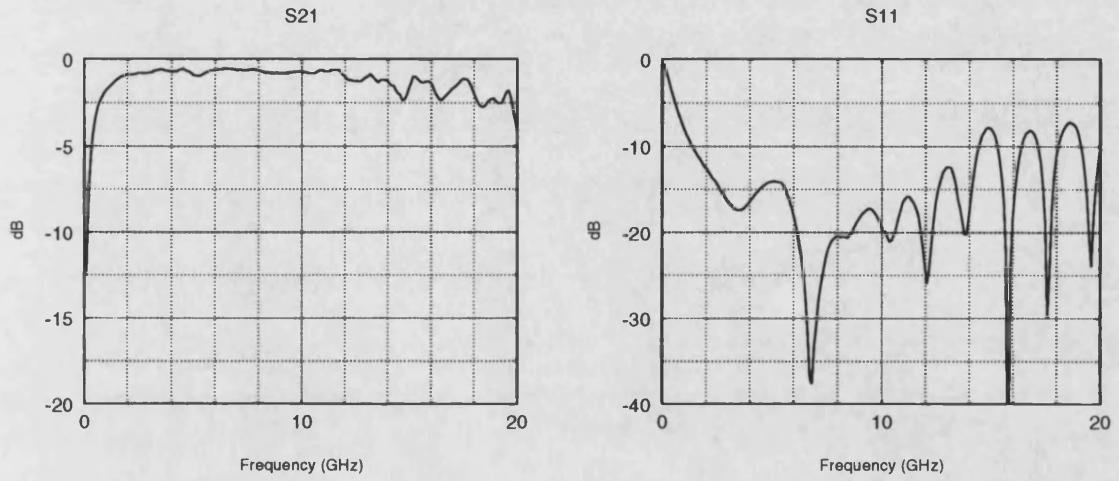

Figure 3.8: Single layer 5.6pF ceramic capacitor mounted in series on a 50Ω transmission line

The overall performance is good, however the low frequency region, below 1.5GHz, is being greatly affected. A larger value capacitance was required, a 56pF capacitor was obtained and the results are shown below

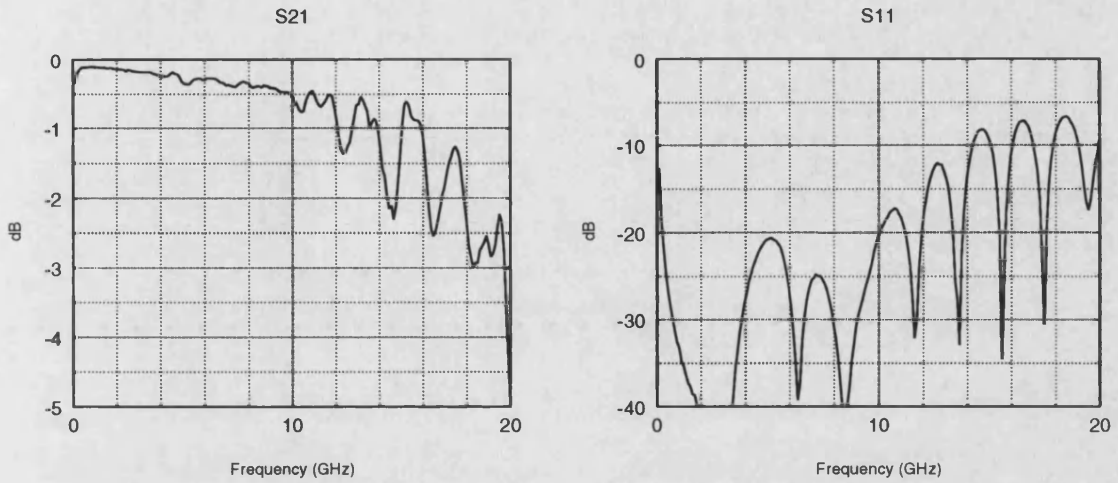

Figure 3.9: Single layer 56pF ceramic capacitor mounted in series on a 50Ω transmission line

The figure shows good performance, from 0.1GHz to 20GHz.

Thus both elements required to form a bias circuit have been implemented, with good performance from 0.1GHz to 20GHz. This allows bias to be applied to multiport devices mounted on microstrip circuit boards.

3.5 Estimation of Parasitics

One of the main features of the measured results in chapter 4 is the large effect that circuit parasitics can have upon the measured performance of devices. "Parasitics" is a general term used to describe unwanted effects associated with microwave devices or circuits. The common parasitic effects are extra fringing capacitance due to the proximity of other structures, extra series inductance due to device interconnects and extra series resistance due to lossy interconnects.

In this work the main parasitic has been found to be series inductance in device connections, it was important for the modelling procedures undertaken in this work to obtain an estimate of this inductance. In order to obtain this estimate two of the tape bond connections used for connecting to the MMICs were connected in series on a 50Ω transmission line, this was then compared with a simple model and an estimate of the inductance obtained. Firstly the 50Ω transmission line was measured as a benchmark for comparison with other measurements, the results are shown below

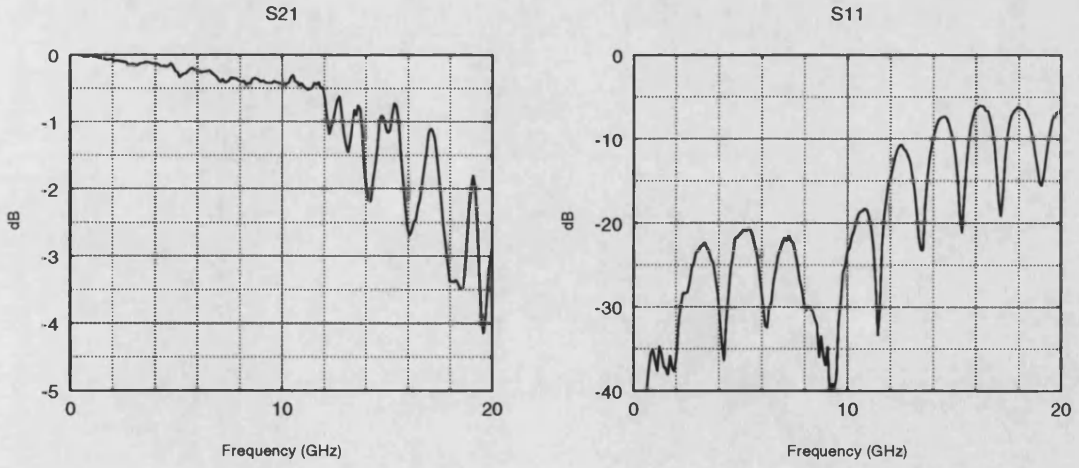

Figure 3.10: S-parameters of a 25.4mm long 50Ω transmission line

The microstrip line is fabricated on high K dielectric ϵ_r=10.5, board thickness=0.635mm, line width=0.59mm. It is seen that the line has good performance up 12GHz, above which

the through transmission rapidly decreases and the reflection coefficient increases. This may well be due to radiative effects, since a free-space wavelength of 25.4mm is equivalent to a frequency of 11.8GHz.

The two tape bonds were then mounted in the line, the measured results are shown below, the through transmission has been normalized to the 50Ω line results above, so that only the response of the tape bonds is shown. The reflection coefficient is unaltered, since it is not a straightforward matter to remove the effect of the transmission line from the results. Together with the measured data the response of a series inductance is shown as modelled by SuperCompact^{TM} at various values

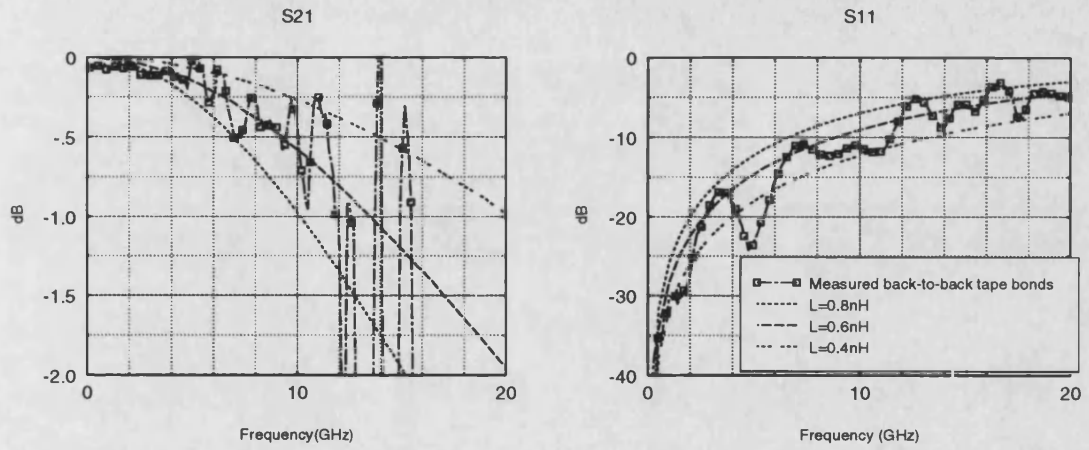

Figure 3.11: Measured and modelled results for two tape bonds mounted in series on a 50Ω transmission line

From these results it was decided to estimate the inductance of a single tape bond as 0.3nH. Thus a good estimate of the inductance of the microstrip to MMIC connections used in this work has been obtained.

In chapter 4 chip resistors are used as matched terminations, it was necessary to estimate the parasitics associated with these elements. The resistors were to be grounded on one side using a through substrate wire bond, in order to assess the performance of this configuration a resistor was mounted on a 50Ω transmission line with one side grounded as described.

The element was modelled on SuperCompact^{TM} as an inductor in series with a resistor, the measured and modelled results are shown below

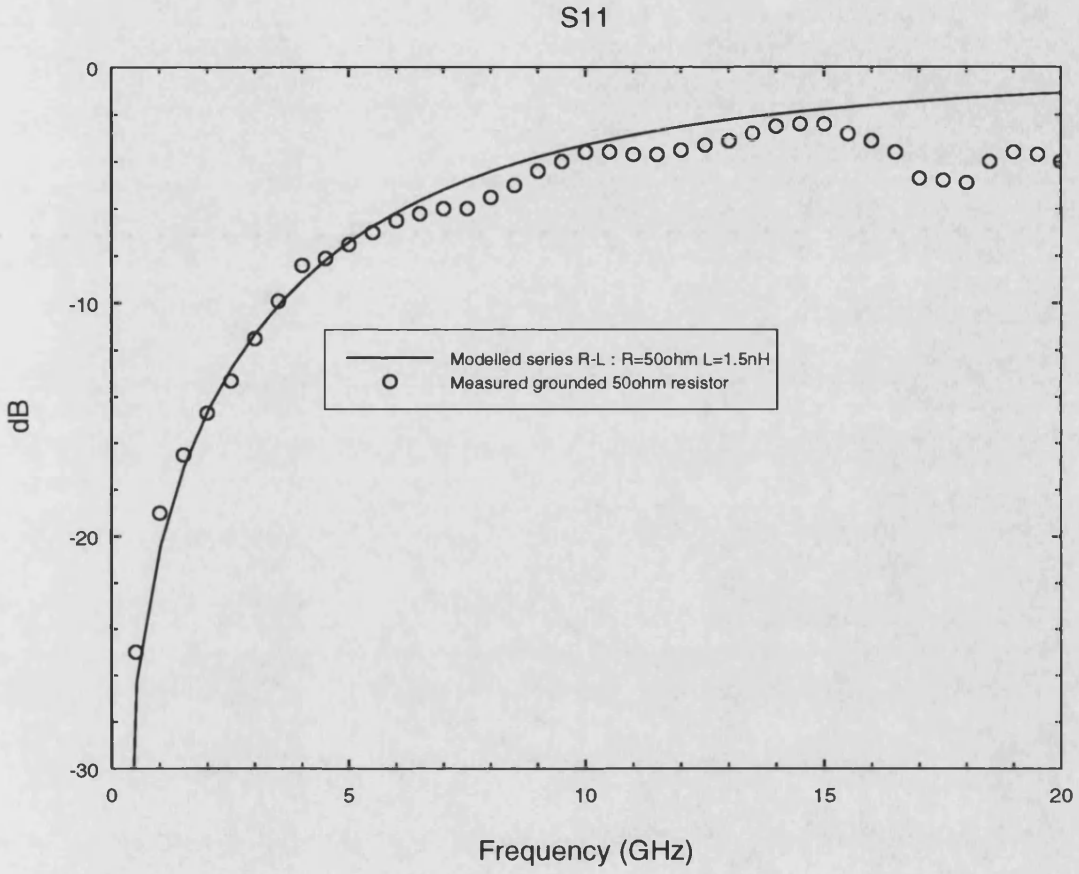

Figure 3.12: Measured and modelled reflection coefficient of a grounded 50Ω chip resistor

These results show that the grounded resistor is modelled very well as a 50Ω resistor in series with and inductance of 1.5nH.

In the third of the chips fabricated as part of this work, resistive termination were fabricated on-chip. These consisted of a 36pF capacitor in series with a 50Ω resistor which was grounded using a through substrate via hole. The performance of these was investigated and the measured results are shown below

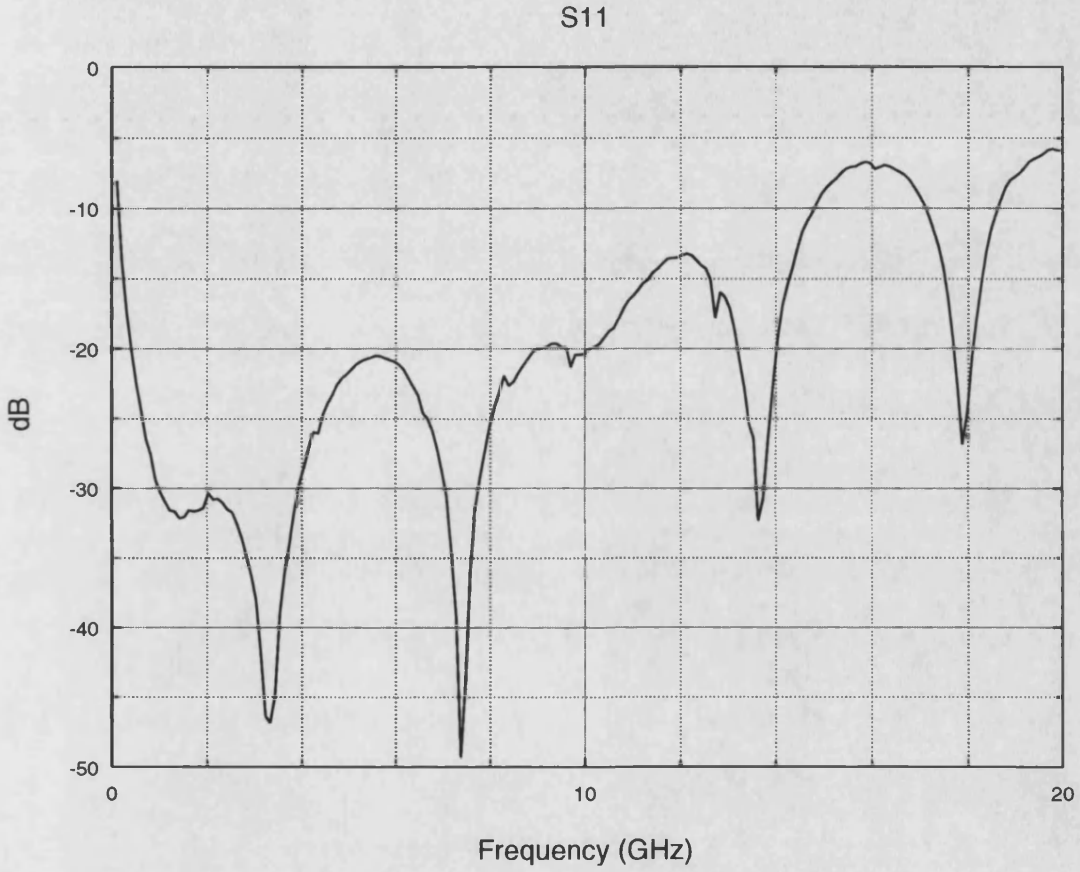

Figure 3.13: On-chip, 36pF capacitor in series with grounded 50Ω resistor

If these results are compared to those of figure 3.9 for a series 56pF single layer ceramic capacitor it seen that the performance is equally good with a reflection coefficient less than -20dB up to 10GHz. The reflection coefficient is slightly higher at low frequency, since the capacitor value is less for the on-chip version. Comparing these results to those for the hybrid chip resistor, shown in figure 3.12, it is seen that the performance is much improved, showing the low level of parasitics associated with MMIC lumped elements.

3.6 Summary

In this chapter a number of issues relating to the measurement of MMICs have been discussed. The mounting fixture used to carry out measurements has been described in detail. Particular problems associated with measuring multiport devices have been discussed, and the errors introduced by mounting MMICs in hybrid microstrip test fixtures have been investigated. Microwave bias circuits have been designed, using chip capacitors and in-house designed choke coils, with good performance from 0.1GHz to 20GHz. The parasitic inductance of the tape bond connections used in this work were estimated and were found to be modelled well be a simple series inductance. Finally, the performance of chip resistors and on-chip resistors have been measured, the on-chip resistors were found to have improved performance over the hybrid chip devices. The on-chip resistor-capacitor combination was found to have performance as good as that of a single layer ceramic capacitor mounted on a microstrip transmission line and terminated in a high precision coaxial load.

Chapter 4

Measured and Modelled Results of Initial Wide FET Structure

4.1 Introduction

The main application for wide FET structures that is investigated in this work is voltage controlled directional coupling. Passive directional couplers have many applications, they are used in communication systems, radar systems and measurement instrumentation. The basic function of a directional coupler is to sample or "couple" power from a transmission line [86]. It is well known that both forward and backward travelling waves exist on transmission lines, it is property of directional couplers that the forward and backward waves are sampled independently [86]. This property makes directional couplers extremely useful in many applications, where the magnitude of forward or backward waves is required. For example one of the fundamental properties of a microwave device is the magnitude of the voltage wave reflected from it, this is readily measured by a directional coupler and this forms the basis of microwave reflectometry[87].

Directional couplers can be designed in any transmission medium, figure 4.1 shows a single section microstrip coupler

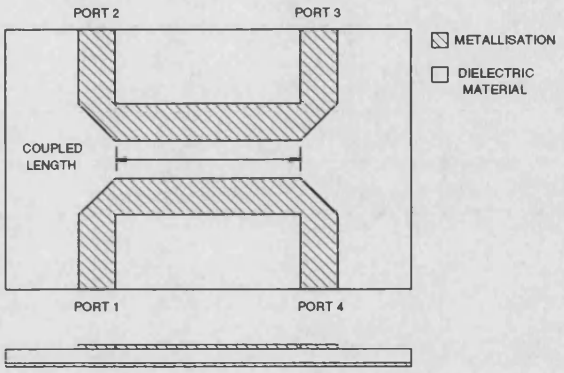

Figure 4.1: A microstrip one section coupler

In such a device power incident on port 1 will be coupled "backwards" to port 2, ideally no power will couple to port 3 and the remaining power will pass to port 4, because of the nature of the coupling this is known as a backward wave coupler. A coupler is characterized by the ratios of the powers at ports 2, 3 and 4 (P_2, P_3, P_4), to that at port 1 (P_1). The ratio P_4/P_1 is known as *through transmission* and the ratio P_2/P_1 is known as the *coupling*. Since no coupler is ideal, a small amount of power will always couple to port 3 and the ratio P_3/P_1 is known as the *isolation*. An important figure of merit for a coupler is the ratio of the coupling to the isolation, this is known as the *directivity*. In this work the *coupling* will be referred to as the *backward coupling* and the *isolation* will be referred to as the *forward coupling*. The mechanism of the coupling has been analysed by many workers and is well understood [37], the method of analysis is similar to that given in chapter 2 but more straightforward, results for such two-line systems will be shown later in the chapter. The backward coupling is not frequency independent and for the single section case, is at a maximum at only one frequency, that is, when the coupled length is equal to a quarter of a wavelength. The backward coupling is in fact a sinusoidal function of frequency, thus a maximum also occurs at odd multiples of a quarter wavelength, however, the fact that losses

however, the fact that losses increase with frequency, means that the first maximum has the greatest magnitude. The bandwidth of the coupler can be increased by using multiple quarter wavelength sections, designed such that the coupling of each section forms a particular profile, Chebychev or Maximally Flat for example.

Voltage controlled couplers have been theoretically investigated by a number of workers. Initial interest was in slow-wave metal-insulator-semiconductor (MIS) transmission lines [88], here it was found that under certain conditions, dependent on device geometry and substrate conductivity, very low wave propagation velocities occur, hence "slow-wave". This led other workers, notably Hughes and White [89] to investigate voltage controlled slow-wave microstrip structures where the phase velocity of the transmission line was controlled by the d.c. bias applied to the line. Hughes and White [89] suggested other applications including voltage controlled coupling, where two MIS lines are brought into close proximity and the coupling coefficient could be controlled by d.c. bias. Coupled MIS lines have been analysed by Itoh [90] and their application as directional couplers was investigated in another work [91]. Schottky contact, rather than MIS transmission lines have been investigated by Jager [26, 92, 93]. In [93] the structure is analysed using the parallel plate waveguide model and experimental results are shown for the bias dependent phase velocity of the line. One of the first analyses of coupled Schottky lines was carried out by Baudrand [94], later he published experimental as well as modelled results for coupled coplanar Schottky lines. Their performance as an isolator was shown, but no variable coupling results shown. Variable coupling for coupled coplanar Schottky lines was presented by Mohammed and Tripathi [95] and by Mohammed [31], theoretical results for devices approximately 2.5mm wide are shown.

Voltage variable directional couplers could have many useful applications, depending on the type of variation obtained these could include

- On chip tunability which would be extremely useful in MMIC applications where first pass success is often a necessity. Tight specifications could be met and process variations corrected for ensuring high yields.
- Variable power splitting and combining.
- If the directivity is controllable then such devices could be used within microwave measurement systems where coupler directivity is often a limiting factor on performance.

In this work, it is believed for the first time, a wide FET structure is configured as a six-port, where the source, gate and drain lines are considered as three coupled microstrip lines. At the outset of the work it was postulated that by varying the depletion capacitances associated with the gate line, which are varied by the d.c. bias applied to the line, the coupling characteristics of the whole structure could be varied, the following chapter will show that this is indeed the case. "Coupling characteristics" implies either forward or backward coupling, that is either the *isolation* or the *coupling* for a standard backward wave coupler, the type of variation eventually obtained is described in detail in this chapter.

In this work a wide FET is considered for the first time as a voltage controlled directional coupler. Three wide FET structures have been fabricated on multi-project wafers, the first through a Science and Engineering Research Council (SERC) initiative and the second and third, through the Eurochip program, all were fabricated at GEC Marconi Materials Technology Ltd (GMMT), UK. The three designs are denoted FET 1, FET 2 and FET 3, in chronological order of fabrication. For each design a number of devices are obtained, the quantity depending on the yield and the number of universities participating in the chip run. This enables a number of devices from each design run to be characterized, a nomenclature is introduced here to differentiate between devices from the same design run : for the first design run, the first chip will be denoted FET 1#1, the second FET 1#2, etc.

The devices have been fully characterized, including d.c. I-V measurements and S-parameter measurements from 0.1GHz to 20GHz. The results from the model developed in chapter 2 will be compared with the measured results. The measurement and modelling aspects of the work were not separate studies, but "interactive", in that modelled results often inspired measurements and *vice versa.* This will be reflected in the structure of the chapter, the development of the model will occur through the chapter as will the improvement in the scope and quality of the measured results.

The structure of the chapter also reflects the nature of MMIC design, in that the turnaround time from circuit layout to actual device measurements can be four to five months. This means that although model predictions may occur at one point in the chapter, actual measurements may not occur till later in the chapter, at which point the model may well have improved dramatically. Thus, whilst trying to maintain the chronological accuracy of the work, the chapter will seek to maintain a logical flow of ideas.

The chapter will begin by presenting two and three passive coupled microstrip line results and comparing these with other work as a check on the inter-electrode capacitance calculations and the three-line modal analysis. The initial test structure will then be introduced and both d.c. I-V and microwave results will be shown. Measurements using improved test fixtures will follow and these will be compared to the basic modelled results. Using the basic model, source and drain electrode dimensions are optimized for minimum forward coupling and the effect of different gate termination investigated. Full six-port S-parameter measurements are then shown which lead to the introduction of gate resistance into the model. The model is then extended to use the multiport connection method, and reasonably good agreement between measured and modelled S-parameters is shown. Finally conclusions to the chapter are made.

4.2 Passive Coupled Microstrip Lines

4.2.1 Introduction

The analysis of a wide FET requires the FET electrodes to be analysed as passive coupled lines, in this work the resistive network analogue technique is used and is outlined in chapter 2. In order to validate this part of the model a number of passive structures were analysed and compared with other theoretical and measured results. In this section the normal mode parameters for a single line, two and three coupled lines will be presented and compared with other workers results. The measured S-parameters for three coupled microstrip lines will be compared with modelled results.

4.2.2 Normal Mode Parameters

Initially a single microstrip line was analysed, the results for characteristic impedance, Z_o and effective dielectric constant, ϵ_{reff} are shown here compared with a SuperCompact^{TM} analysis using the Bryant and Weiss method [96]

	Z_o (Ω)	ϵ_{reff}
This work	50.2	1.95
SuperCompact^{TM}	49.95	1.95

Table 4.1: Propagation characteristics of a microstrip line

The microstrip dimensions were : H=0.787mm, W=2.4mm ϵ_r=2.3 and enclosure height, H_u=80mm, the table shows very good agreement.

The two coupled line case was then analysed, figure 4.2 shows the configuration.

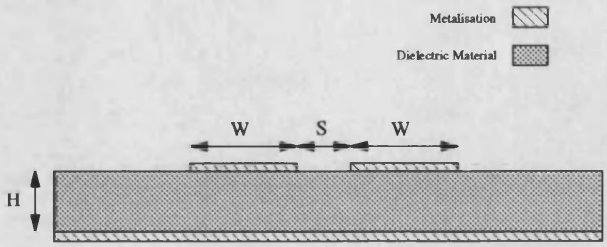

Figure 4.2: Two coupled microstrip lines

Two symmetrical, coupled lines give two mode impedances, the even mode, Z_{oe} and the odd mode, Z_{oo}, a comparison of various results is shown below

	Mode Impedance(Ω)					
	W/H=0.2, S/H=1		W/H=0.5, S/H=1		W/H=0.1, S/H=0.2	
	Z_{oe}	Z_{oo}	Z_{oe}	Z_{oo}	Z_{oe}	Z_{oo}
Bryant & Weiss [96]	104.9	78.7	77.4	57.7	156.0	66.1
Garg & Bahl [97]	107.0	74.0	78.9	57.9	-	-
El-Deeb [59]	101.3	75.4	74.7	55.5	146.7	59.0
This Work	102.1	77.7	76.7	57.4	145.7	63.75

Table 4.2: A comparison of mode impedances for two symmetrical coupled microstrip lines (H=0.635mm ϵ_r=9.6)

The above results show good agreement with other work that has used different analysis techniques, [96] used a Green's function method to calculate the inter-electrode capacitances, [97] used empirical expressions to define the capacitances and also good agreement is seen between work using similar techniques as in [59].

Having obtained this agreement the analysis was extended to the unsymmetrical two line case. In the case of unsymmetrical lines the power no longer splits evenly between the two modes and the mode voltage ratios are no longer unity as for two symmetrical lines [37]. Also four different mode impedances are defined, one for each mode, on each line. A comparison is shown below

	Mode Impedance (Ω)				Mode Voltage Ratio			
	Even Mode		Odd Mode		Even Mode		Odd Mode	
	line 1	line 2	line 1	line 2	line 1	line2	line 1	line 2
This Work	63.7	39.1	44.7	27.4	1.0	1.11	1.0	-0.55
Tripathi [47]	63.1	38.8	43.73	26.9	1.0	1.093	1.0	-0.56

Table 4.3: A comparison of mode impedances and mode voltage solutions for two unsymmetrical coupled microstrip lines. Dimensions : H=0.635mm, W_1=.6mm, W_2=1.2mm, S=0.4mm ϵ_r=9.7

Again very good agreement is obtained.

The analysis was then extended to the three line case, initially electrically identical lines were analysed, this produces just three mode impedances, these are shown below with comparison

	Mode Impedance		
	Mode a - Odd	Mode b - Even	Mode c - Bulk
This Work	49.8	81.5	31.1
Pavlidis & Hartnagel [60]	50.0	78.4	30.0

Table 4.4: Mode impedances of three symmetrical microstrip coupled lines. Dimensions : $W_{1,2,3}$=.432mm, $S_{1,2}$=.19mm, H=.635mm ϵ_r=9.8

Reasonable agreement is shown here, the analysis in [60] assumes that lines of equal width will produce equal mode impedances this has been shown not to be the case [98], it is possible that these assumptions cause the discrepancies seen above.

The analysis was then extended to the general unsymmetrical case of three different line widths and two different gaps the results and comparison are shown below

	Mode Impedance (Ω)								
	Mode a - Odd			Mode b - Even			Mode c - Bulk		
	line 1	line 2	line 3	line 1	line 2	line 3	line 1	line 2	line 3
This Work	73.5	54.9	29.1	46.08	33.04	20.37	104.8	71.46	39.71
Tripathi [61]	76.5	57.0	30.0	46.5	35.5	19.5	106.5	73.5	40.5

Table 4.5: A comparison of mode impedances for three unsymmetrical coupled microstrip lines. Dimensions : H=0.635mm, W_1=0.3mm, W_2=0.6mm, W_3=1.2mm S_1=0.2mm, S_2=0.4mm ϵ_r=9.8

	Mode Voltage Ratios								
	Mode a - Odd			Mode b - Even			Mode c - Bulk		
	line 1	line 2	line 3	line 1	line 2	line 3	line 1	line 2	line 3
This Work	1.0	0.597	-0.667	1.0	-0.889	0.172	1.0	1.165	1.15
Tripathi [61]	1.0	0.6	-0.66	1.0	-0.875	0.175	1.0	1.187	1.125

Table 4.6: A comparison of mode voltage ratios for three unsymmetrical coupled microstrip lines. Dimensions : H=0.635mm, W_1=0.3mm, W_2=0.6mm, W_3=1.2mm S_1=0.2mm, S_2=0.4mm ϵ_r=9.8

	Propagation Constant, β		
	Mode a - Odd	Mode b - Even	Mode c - Bulk
This Work	2.47	2.35	2.75
Tripathi [61]	2.48	2.36	2.76

Table 4.7: A comparison of propagation constant for three unsymmetrical coupled microstrip lines. Dimensions : H=0.635mm, W_1=0.3mm, W_2=0.6mm, W_3=1.2mm S_1=0.2mm, S_2=0.4mm ϵ_r=9.8

Tables 4.5, 4.6 and 4.7 show mode impedances, mode voltage ratios and propagation constants obtained for the general case and good agreement is again obtained.

Finally the structure of a wide FET was analysed and the mode impedances obtained, these were compared with a SuperCompact^{TM} two line analysis which ignored the presence of the gate line

	Mode Impedance (Ω)								
	Mode a - Odd			Mode b - Even			Mode c - Bulk		
Line No.	1	2	3	1	2	3	1	2	3
This Work	34.53	INF	34.53	7.48	78.8	7.48	132.4	1394.5	132.4
SuperCompact^{TM}	33.7	-	33.7	-	-	-	132.1	-	132.1

Table 4.8: A comparison of mode impedances for a wide GaAs FET structure. Dimensions : H=200μm, Source and Drain, W_1=W_3=30μm, Gate, W_2=1.2μm S_1=S_2=5μm ϵ_r=12.9

Table 4.8 shows the six independent mode impedances obtained from a symmetrical structure where lines one and three have the same width. Where comparisons are possible good agreement is obtained. The finite level of the other mode impedances show the importance of including the effects of the central line, even in this case, where the width of line two is a very small fraction of the other lines.

Thus the normal mode parameters: mode impedance, mode voltage ratio and propagation constant, have been calculated for the single, two coupled and three coupled line cases and compare well with other work. These are now used to calculate the S-parameters of three coupled microstrip lines, this will be presented in the next section.

4.2.3 Measured and Modelled S-parameters of Three Coupled Microstrip Lines

To validate the modal analysis used to obtain the S-parameters from the normal mode parameters, the S-parameters of a number of three coupled line circuits were measured and compared with modelled data.

A schematic of the first microstrip circuit is shown in figure 4.3 and will be denoted circuit 1

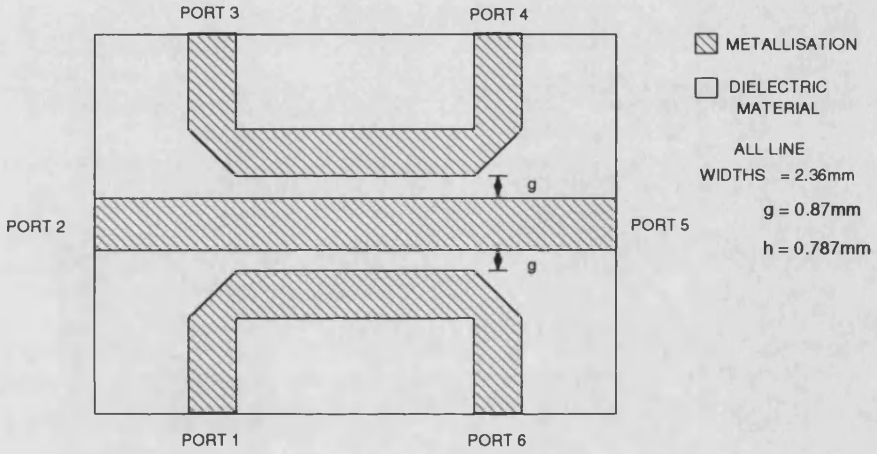

Figure 4.3: Three symmetrical coupled lines

The measured and modelled data for nearest lines is shown in figure 4.4

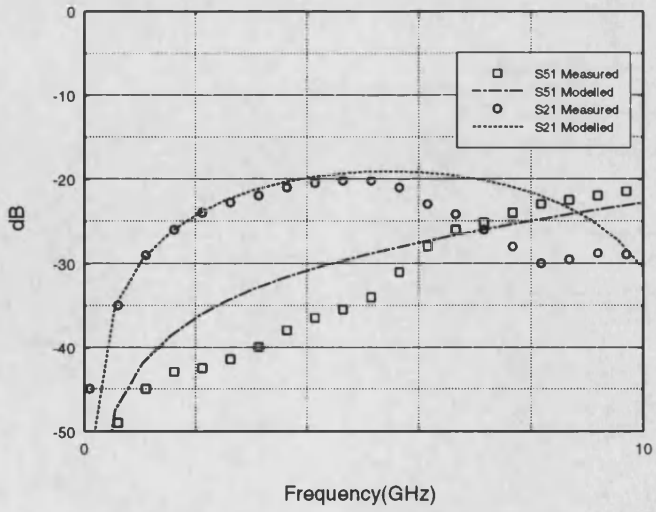

Figure 4.4: Forward and backward coupling for lines 1 and 2 of circuit 1

The model used an effective coupled length of 10.0mm, slightly longer than the actual physical length of 9.5mm, this accounts for end effects at the corners of the outer lines. It is seen that good low frequency agreement is obtained for the backward coupled response, S_{21}, the agreement is less good at higher frequencies, this is most likely caused by dispersion, that is the variation in the mode impedance and propagation constant with frequency, this is not being accounted for in this model. The forward coupling or isolation, S_{51} has reasonable agreement across the whole band, the most likely cause for the difference observed is the finite reflection from the connectors at the output of the transmission lines. As discussed in chapter 3, the phasor addition of the reflected signal with the true isolation signal can cause large variations, especially when these two signals are of the similar magnitudes. An important feature that the model predicts is the change from backward coupling at lower frequencies to forward coupling at higher frequencies. In symmetrical two coupled line circuits this effect is primarily caused by the difference in the propagation constants for the even and odd modes, in three coupled line circuits, the analysis is more complex and all the normal mode parameters can affect the S-parameters.

The measured and modelled data for the outer lines is shown below

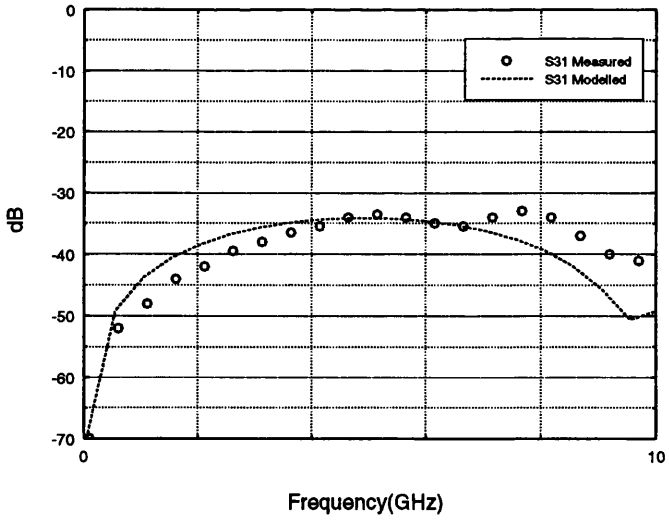

Figure 4.5: Backward coupling for lines 1 and 3 of circuit 1

Here the agreement for backward coupling, S_{31} is reasonable. The forward coupling or isolation results, S_{41} are not shown since being at even lower levels than S_{51} in figure 4.4

they are more prone to errors caused by the finite reflections from the mitred bends and from from the connectors at the output of the transmission lines. These problems will be less important when modelling wide FET structures since the line spacings are typically much smaller, resulting in much higher levels for both backward coupling and isolation.

The wide FET structures to be investigated will initially be configured such that the gate line is open circuited with respect to microwave signals. Thus any model must be able to open circuit the central line, in order to check this part of the model, a second circuit (circuit 2) shown in figure 4.6 was fabricated, measured and modelled results are shown in 4.7

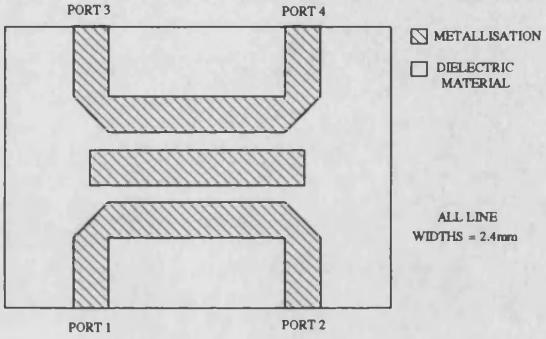

Figure 4.6: Three coupled microstrip lines with a central open circuited line

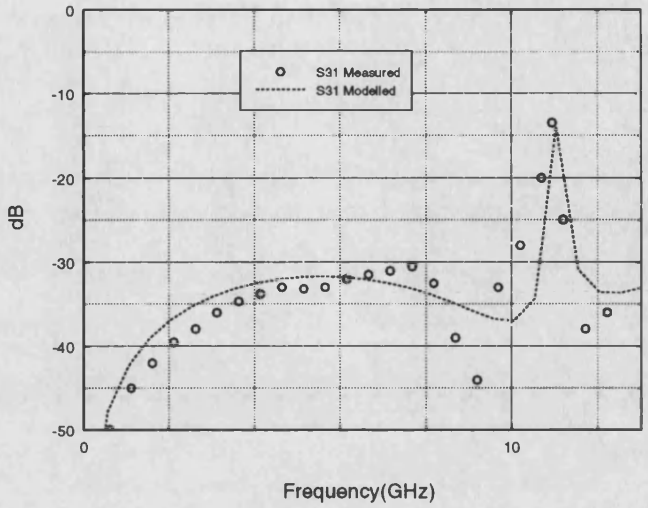

Figure 4.7: Measured and modelled S-parameters for three microstrip lines with a central open circuited line

The main feature of these results is the sharp resonance around 11GHz, this is caused by the half wavelength resonance of the central open circuited line. The resonant frequency is being predicted reasonably accurately, this frequency is very dependent on the choice of coupled length. The coupled length, however, is difficult to estimate because of fringing effects both at the corners of the outer lines and at the ends of the microstrip line. For the model shown here the effective coupled length was set to 10.5mm, this is 1.0mm longer than the physical length of the central line which was 9.5mm. This is the standard effect of fringing, whereby open circuit lines are modelled as the physical length plus a short length of line to model the fringing capacitance [37].

The wide FET structure has equal outer line widths, but a much thinner central gate line, in order to check the model a microstrip circuit of similar configuration was fabricated. A schematic of the circuit (circuit 3) is shown in figure 4.8

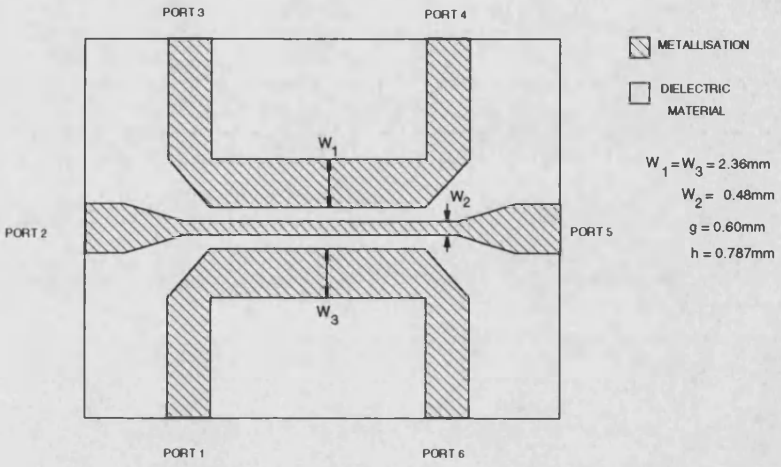

Figure 4.8: Three coupled microstrip lines $W_1 = W_3 \neq W_2$

The tapers on the central line are used to obtain the best match from the high impedance central line to the 50Ω terminations used for S-parameter measurement. The measured and modelled results are shown overleaf for lines 1 and 2

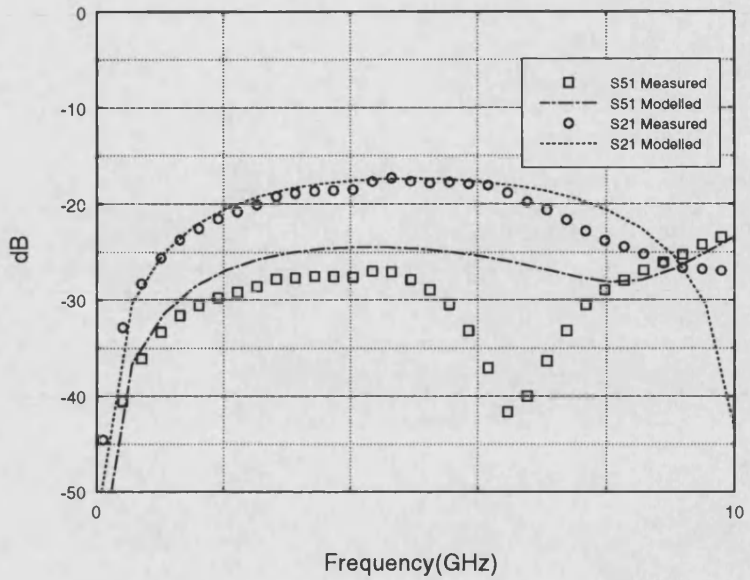

Figure 4.9: Backward coupling for lines 1 and 2 of circuit 3

Again, as in the circuit of figure 4.2 good agreement is obtained for S_{21}. The isolation is again being affected by reflections as in figure 4.4, possibly more so in this case because of the tapers on the central line.

Results for lines 1 and 3 are shown below

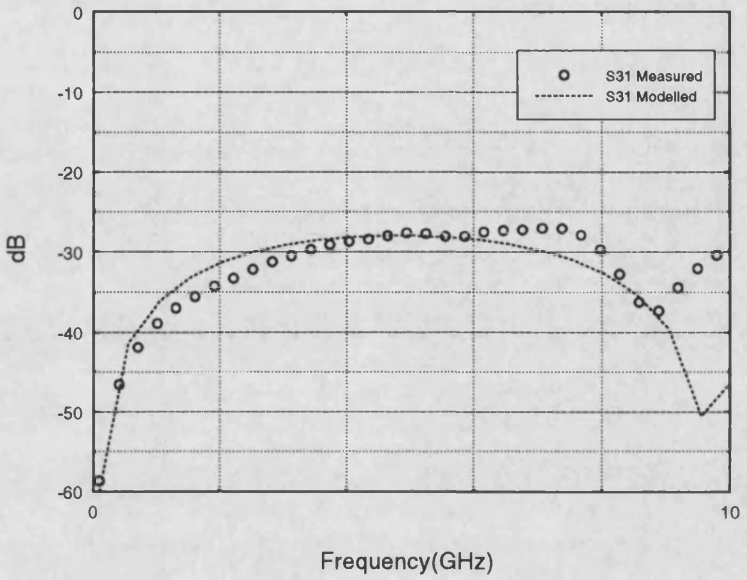

Figure 4.10: Backward coupling for lines 1 and 3 of circuit 3

For backward coupling, S_{31}, reasonable agreement is obtained.

Thus these measurements show that within the range of measurement error introduced by the test fixture, mitred bends and tapered lines, the model predicts the performance of three coupled microstrip lines reasonably well.

4.3 Initial Wide FET Structure

4.3.1 Introduction

In this section the first of three wide FET structures will be studied. The first device was designed prior to the commencement of this work. It was designed using standard foundry devices, configured to give a large gate width. The width of the device was chosen such that variable coupling effects might be observed in the range of the measurement instrumentation available, that is 0.045GHz to 20.3GHz. As discussed in the preceding section, for coupled microstrip lines, maximum backward coupling is observed at a frequency such that the coupled length is one quarter of a wavelength. It was felt that the device should be long enough for maximum coupling to be observed, thus a quarter-wave frequency of 18GHz was chosen, this corresponds to approximately 1.5mm coupled length for microstrip on GaAs. Whilst a lower frequency would be desirable in terms of measurement accuracy and lower parasitic effects, it would require a longer device, and the yield of these devices will tend to decrease with device length. This is because the yield is dominated by the gate line, the gate has a length of 0.7μm and a width of 1500μm, to maintain the integrity of the gate across this length of wafer is extremely difficult. One of the main reasons for this is that approximately each 200μm^2 of wafer is defined by a separate mask [99], thus for a 1500μm gate length 6 - 7 masks might be required, each of which must be accurately aligned, thus if two adjacent masks are misaligned by 0.35μm then the gate could become open circuit. Thus a width of 1500μm for the gate was the best compromise between, yield and measurement considerations.

The chip was fabricated at GEC-Marconi Materials Technology Ltd(GMMT), Towcester, England, using the F14 process and was part of a Science and Engineering Research Council (SERC) initiative which gave academic institutions access to GaAs foundry facilities. A schematic of the layout of the chip is shown below

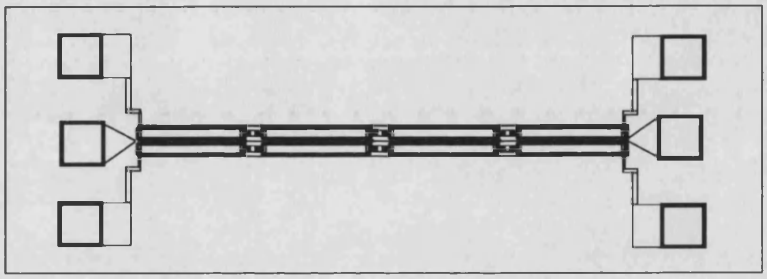

Figure 4.11: Initial wide FET test structure : FET 1

The chip measures 2180μm by 938μm and the device is based on the GMMT standard 300μm wide, 0.7μm gate length device. In order to obtain a gate width of 1500μm, four such devices were connected in parallel. Each 300μm section is connected by two M2 - M3 via holes, these are required to maintain the maximum aspect ratio for a gap on any layer of 50:1 [24]. In this case the source to drain spacing is $\simeq$10μm, two 300μm FETs in parallel would produce a gap 600μm by 10μm, violating the design rule, thus 300μm sections were used. The inclusion of these vias means that the structure no longer has a uniform cross-section in the direction of propagation, this was one of the assumptions made in chapter 2. However, since the dimensions of the vias are very much smaller than a wavelength, they are initially assumed to have no effect, it will be seen from the results in this chapter that this is a reasonable assumption.

In figure 4.11 it is seen that each of the lines has a square bond pad at either end, these are 120μm square and are initially wire bonded to the microstrip lines of the MMIC test fixture. The detailed cross-sectional geometry of the device will be discussed later in the section.

In this section the d.c. characteristics of FET 1 are measured and compared with foundry data. Initial measurements showing the variation of device S-parameters with gate bias level are shown, further results using improved test fixtures are then discussed and compared to modelled results. The model is then used to predict optimum source and drain line dimensions for minimum forward coupling and the effect of different gate line terminations is investigated. Full six-port S-parameters are presented at various bias levels and compared with modelled results, this leads to a number of improvements in the model. The model is then fitted to the measured six-port data and reasonably good agreement is obtained. Finally some conclusions are drawn.

4.3.2 D.C. Characterization and Measurement for FET 1

In order to check the basic functionality of the devices the I-V characteristics of two devices were measured. These measurements would show whether transistor action was being obtained, also a number of important d.c. parameters can be calculated from the curves, these are compared with manufactures data for similar devices. The results for two devices are compared to assess repeatability from device to device.

For d.c. testing the chips were mounted in a microwave test fixture, this reduced the number of mounting operations required to fully characterize the devices, the test fixture will be discussed in detail in the next section. The FET was configured in common source mode, drain - source current was applied through a 100Ω resistor and the gate was biased through a 100KΩ chip resistor. The two devices measured were FET 1#3 and FET 1#7, the output I-V curves and the transfer characteristics for the the two devices are shown below

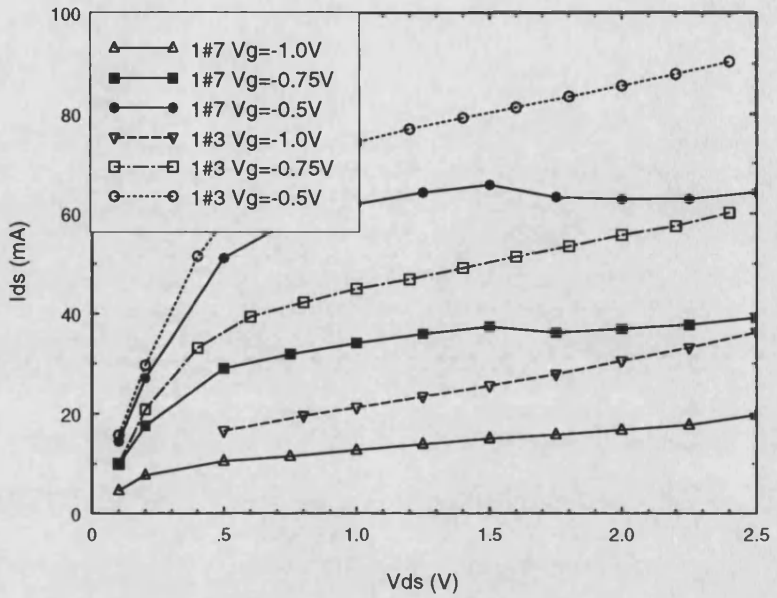

Figure 4.12: Output I-V characteristics for FET 1#3 and FET 1#7

These are typical FET output characteristics [75], showing the "knee" at the transition from the ohmic to the relatively constant output current region. This graph shows that transistor action is being obtained. The two devices' characteristics differ quite substantially, but as will be seen from other results the performance is similar to that suggested by the manufacturers data sheets [24]. From the output characteristics the output resistance of the FET can be calculated, this is shown in table 4.9, measured at V_{ds}=1.5V, V_{gs}=-0.5V. It is interesting to note that above 1.5V V_{ds} FET 1#7 shows a negative slope, although this might suggest a negative differential resistance it is in fact caused by thermal effects in the channel [100]. The other important d.c. parameters are obtained from the FET transfer characteristics, these are plotted overleaf

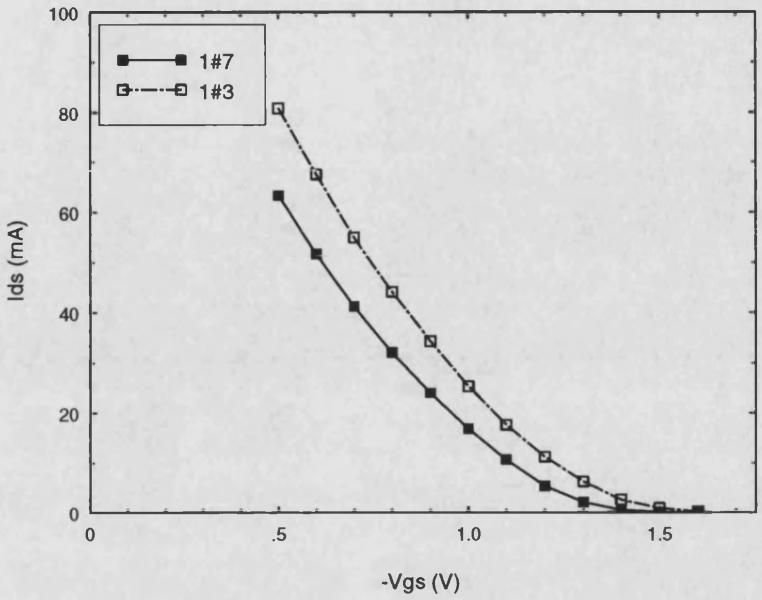

Figure 4.13: Transfer I-V characteristics for FET 1#3 and FET 1#7

These results were taken at constant V_{ds} of 1.5V. Again differing results are obtained. From these graphs the d.c. transconductance, g_m is obtained as the ratio of I_{ds} to V_{gs}. Also an estimate of the maximum drain-source current, I_{dss} can be made by extrapolating the curves to $V_{gs} = 0.0V$. Finally the pinch-off voltage,V_p is found where $I_{ds} = 0.0mA$, this is the gate voltage required to "close" the channel. These parameters are shown below compared with manufacturers data for a single 300μm device

	GMMT 1 X 300μm			Wide FET 1 : 4 X 300μm	
	min.	typ.	max.	FET 1#3	FET 1#7
I_{dss} (mA)	30	45	60	134	117
g_m (mS)	20	30	40	100.8	95.5
R_{ds} (Ω)		640		100	150
V_p (V)	-1.2	-1.8	-2.5	-1.57	-1.45

Table 4.9: D.C. parameters of FETs 1#3 and 1#7 compared with GMMT data

These results are consistent with the fact that the wide FET is four times the width of the 1 X 300μm FET, in that there is approximately four times the maximum current, I_{dss} as one would expect and also approximately four times the transconductance, since transconductance is also proportional to gate width. The output resistance is also consistent, showing

the effect of four devices in parallel as a reduction by approximately four. The pinch-off voltage is within the range specified, and should not be greatly effected by the gate width. The two devices measured show reasonable consistency within the ranges specified by the manufacturers.

Thus the d.c. characteristics for two devices from the FET 1 design have been shown, although important in amplifier design, these parameters are less so in low power, switching-type applications such as those to be investigated in this work. However, they do serve to show that the FETs are functioning as transistors and the gate voltage is controlling the characteristics of the channel region, which is of prime importance in this work. They also show the the devices are typical of those produced by the foundry and therefore will be useful guides to the typical performance obtainable in the various applications investigated. Having completed the d.c. characterization, microwave characterization is presented in the next section.

4.3.3 Initial Voltage Controlled Results

In this section the FET 1 design is characterized at microwave frequencies. The MMIC chip is mounted in a microstrip test fixture to facilitate measurement on an HP8510B network analyser. A schematic of the test fixture is shown here

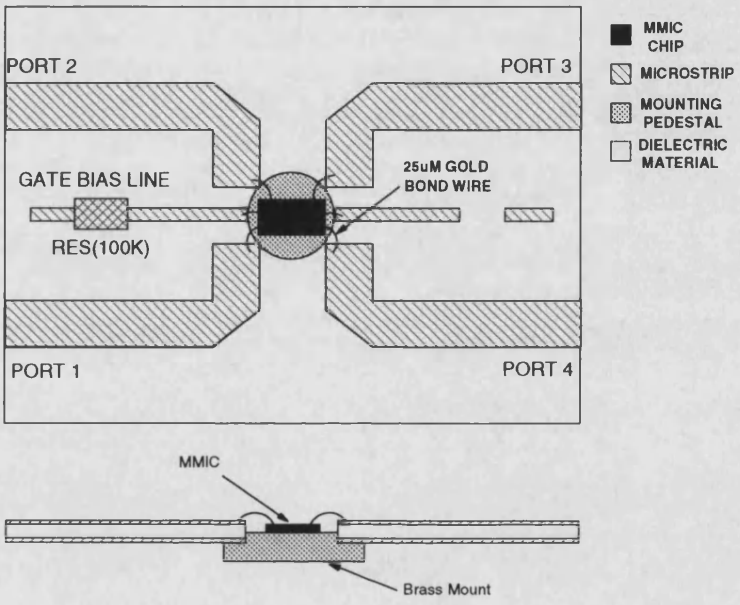

Figure 4.14: An MMIC microstrip mounting circuit

This is a 0.787mm thick, 1 inch square, RT-Duroid^{TM} board with $\epsilon_r = 2.2$. The microstrip lines are 50Ω width, W=2.4mm. The chip is soldered to the brass pedestal and wire bonded with 25μm gold wire from the device bond pads shown in figure 4.11 to the microstrip lines. The duroid circuit is then mounted on an aluminium carrier to which SMA connectors are attached. The SMA connectors are modified such that as well as contacting to the microstrip line they also make pressure contact to the microstrip board, grounding the underside metallization of the duroid to the aluminium carrier, details of this configuration are discussed in chapter 3. A detailed view of the MMIC area of the mounting circuit is shown overleaf

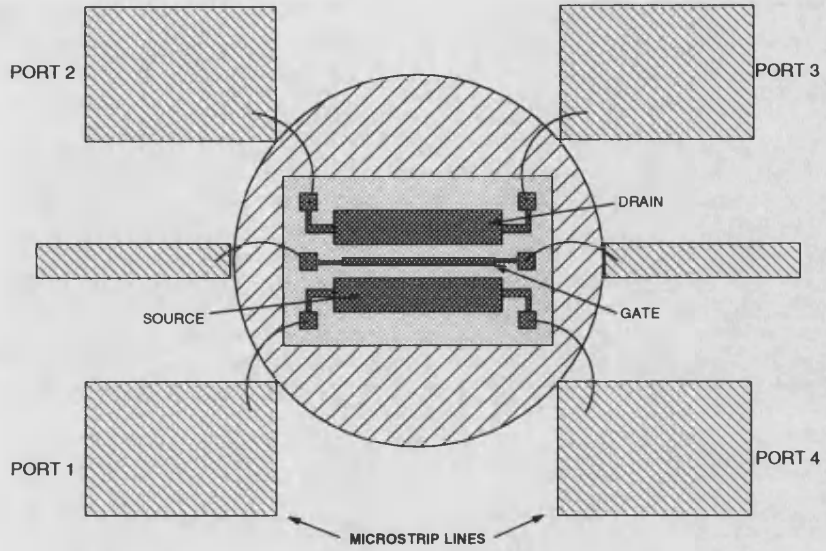

Figure 4.15: A detailed view of an MMIC microstrip mounting circuit

The device is configured as a four-port in order to investigate the variable coupling effects between the source and drain electrodes produced by varying the bias applied to the gate line. The gate is biased through a 100KΩ chip resistor. The device used for these measurements is FET 1#3. The S-parameters of the device were measured initially with no gate bias, and the three important parameters for directional couplers of backward coupling, S_{21}, forward coupling, S_{31}, and through transmission, S_{41}, are plotted logarithmically in figure 4.16. Initially the measurements are shown above 10GHz only, as these show the most interesting results and at this stage the lower frequency results showed no directional coupler properties

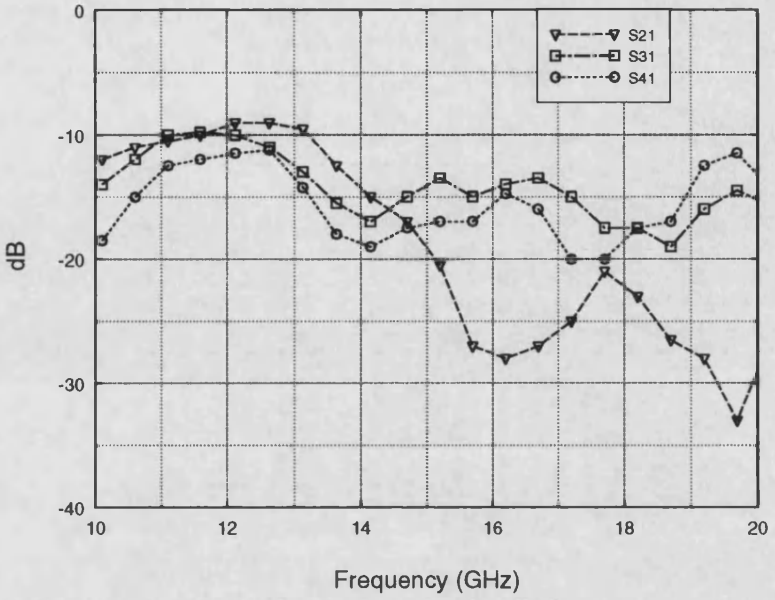

Figure 4.16: S-parameters for FET 1#3 with no gate bias

The first point to note here is that directional coupling has been obtained across a large frequency band, $\simeq$ 15GHz - 20GHz. This is centred around the quarter-wave frequency as discussed earlier. However, backward coupling is not being observed, as in the case of two and three coupled microstrip lines, in fact forward coupling is being exhibited i.e. $|S_{21}| < |S_{31}|$ (linear). However, this is a much more complex device as is seen in chapter 2 where the development of the model is discussed and simple assumptions based on passive three-line circuits are no longer valid. The effect of circuit parasitics must also be taken into account as discussed in chapters 2 and 3. However, all the measurements in this section use first iteration test fixtures which are far from ideal, and are included to show the early stages in the development of this work. The other important point to note from figure 4.16 is that the through transmission is less than the forward coupling, the opposite of this true for standard directional couplers. Also the level of the through transmission is very low, typically for a microstrip coupler at these frequencies with reasonably tight coupling, e.g. -6dB then S_{41} would be of the order of -0.5dB [101], although this device would not be expected to have this performance, levels of -15dB would be unacceptable in any application. The reason for these discrepancies will become clear as the section progresses.

Having obtained the unbiased S-parameters for the device, the gate bias was applied to the device and the S-parameters measured, only negative gate biases are applied since forward bias could result in high gate currents which would damage the gate structure. The results for four different reverse biases for forward coupling, S_{31} are shown below

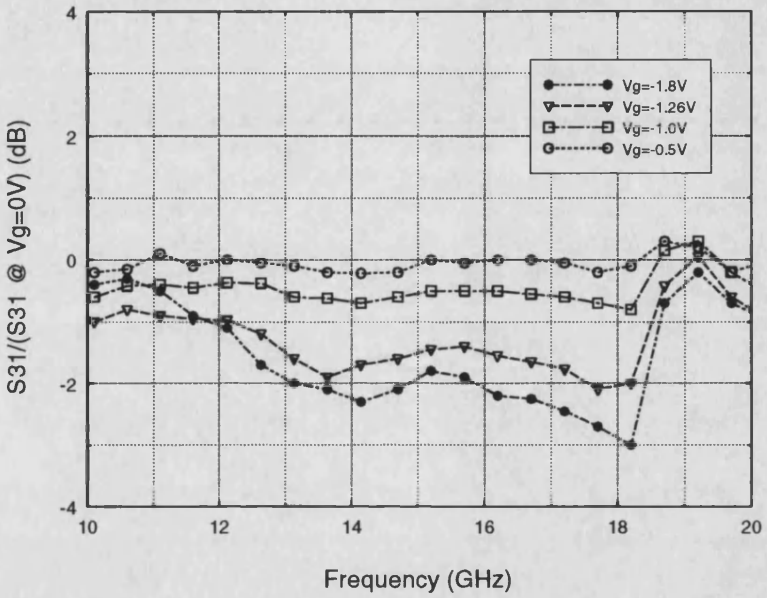

Figure 4.17: Variation in S_{31} for FET 1#3 with gate bias

The graph shows normalized variation, that is, referenced to the zero bias results. Figure 4.17 shows that between 2dB-3dB of variation is obtained, this is reasonable considering that a 3dB change is 50% in terms of actual power level. The variation of the other two important transmission parameters are shown overleaf

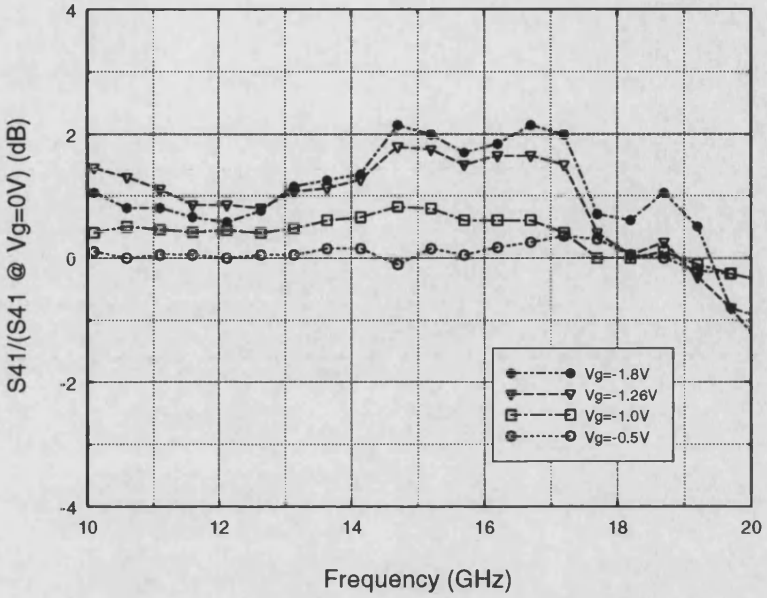

Figure 4.18: Variation in S_{41} for FET 1#3 with gate bias

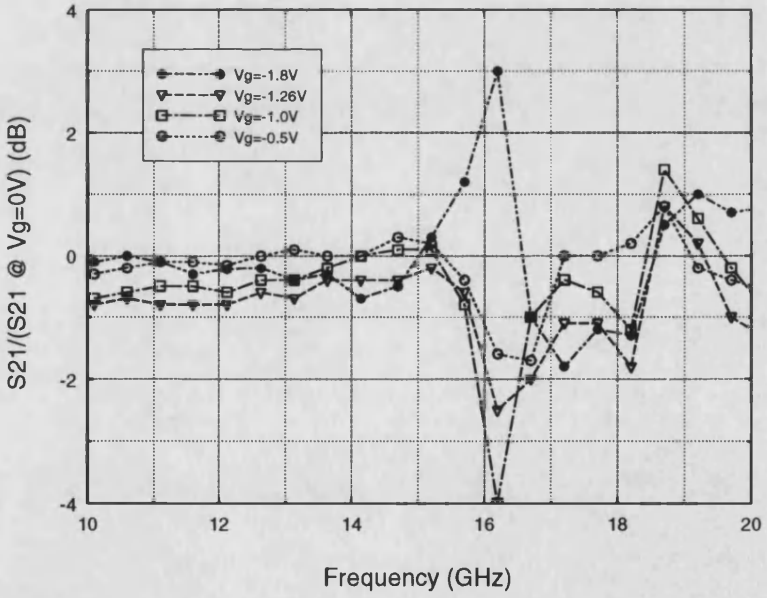

Figure 4.19: Variation in S_{21} for FET 1#3 with gate bias

Figure 4.18 shows the through transmission, it is seen to be increasing with reverse bias, the opposite of the forward coupling in figure 4.17, thus power is being switched from port 3 to port 4, this would seem to be the simple low frequency switching that would be expected for the FET, however in this case there is also directional coupling occurring, in that port 2

remains isolated, in fact figure 4.19 shows that the backward coupling decreases with reverse bias for most frequencies across the band, apart from a sharp resonance in the centre of the band at -1.8V gate bias.

Thus these results show that directional coupling is obtained from a wide FET structure, the coupling is of a forward wave nature. The level of this coupling is controllable by the gate bias, the forward coupling decreases with gate bias, whilst the through transmission increases and the forward coupling decreases for most frequencies with reverse bias. The main drawback to these results is the low level of the through transmission, the following results are attempts to improve the level of the through transmission whilst maintaining the voltage controlled directional coupling properties of the device.

Improvements in Through Transmission of a Wide FET

It is well known that adding lumped capacitors at the end of the coupled region can improve the directivity of two line microstrip couplers [102]. It was felt that the capacitors may also increase the through transmission, since they would tend to short circuit resistive losses between gate to drain and gate to source. Thus, chip capacitors, C = 1pF, were obtained with reasonable microwave performance and added to the circuit as shown below

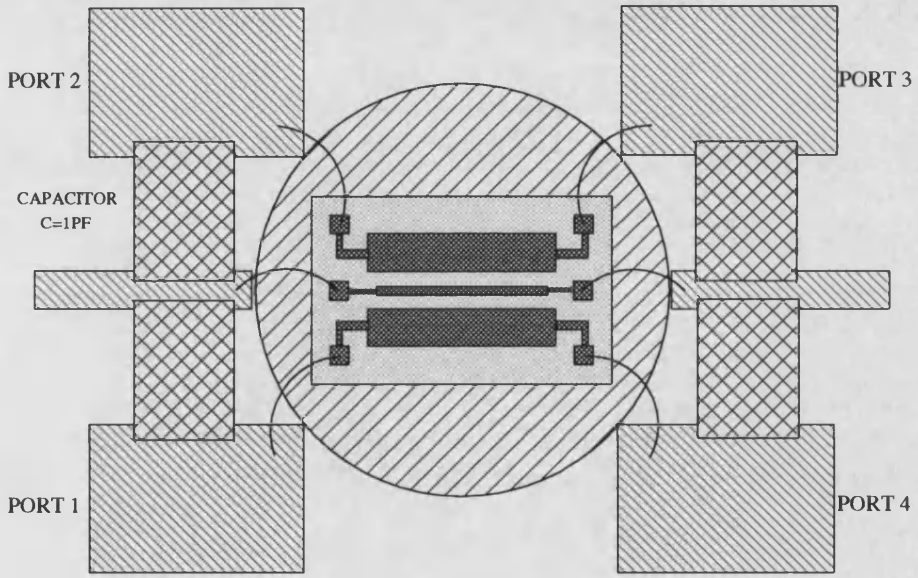

Figure 4.20: Chip capacitors added to basic mounting circuit

This circuit was then characterized as before, the S-parameters are shown below

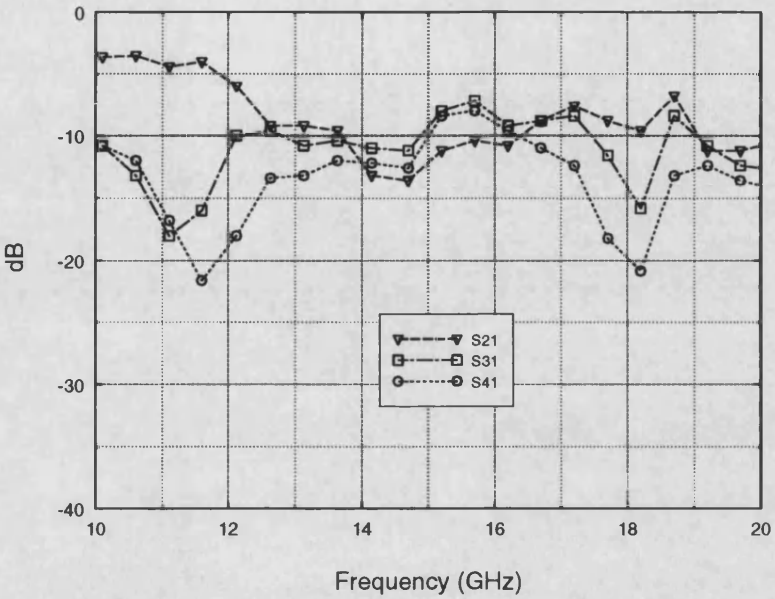

Figure 4.21: S-parameters for FET 1#3 with added capacitors

If these results are compared with figure 4.17, it is seen that as anticipated, the level of the through transmission, S_{41} has increased, however, so too have the backward and the forward coupling. The large band of low backward coupling is no longer present and in fact the through transmission is now at the lowest level.

In an attempt to increase only the through transmission, the capacitors connecting the gate to ports 2 and 3 were removed. The results for this configuration are shown below

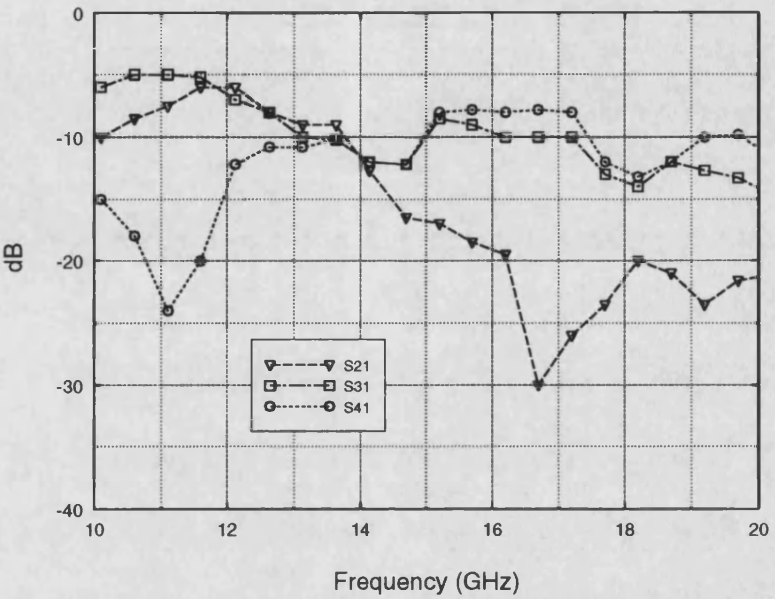

Figure 4.22: S-parameters for FET 1#3 with only two added capacitors

Figure 4.22 shows a dramatic improvement on the results with four capacitors, also comparing with figure 4.17 a large improvement is observed. From 14GHz the through transmission is greater than the forward coupling as expected for a standard directional coupler. The level of the through transmission is also much improved, at best it is -7.8dB. The backward coupling is also low resulting in directivities between 6dB-20dB from 14GHz-20GHz. However, as is often the case, these improvements in basic performance have been offset by a decrease in the amount of variation with gate bias, this has been reduced to $\simeq$1dB, for both forward coupling and through transmission.

The MMIC containing the FET 1 design also contained other circuits, the wide FET was not central on the chip and thus was not mounted centrally on the pedestal, this resulted in substantially longer bond wires on one side of the device. The longer bond wires were connected to ports 1 and 4, this explained the high through transmission obtained for the device. Thus another chip was cleaved such that the wide FET could be measured in isolation. FET 1#11 was cleaved, and the wide FET was mounted centrally, with as short as possible bond wires to minimize their effect. The S-parameter measurements are shown below

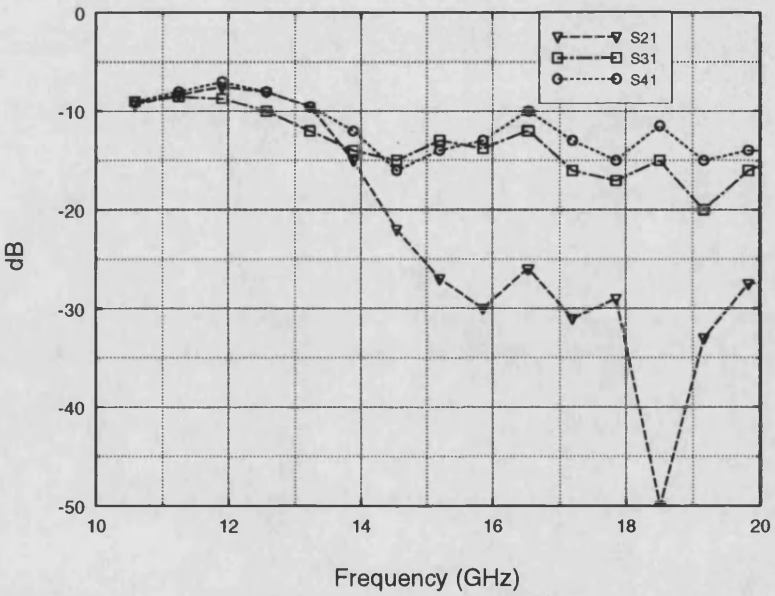

Figure 4.23: S-parameters for FET 1#11 mounted centrally

There is seen to be a marked improvement compared with the original measurements in figure 4.17. The basic device, with no additional capacitors, gives through transmission greater than forward coupling and low backward coupling from 15-20GHz, resulting in directivities of between 10-30dB.

The voltage variable results were also repeated, forward coupling is shown below

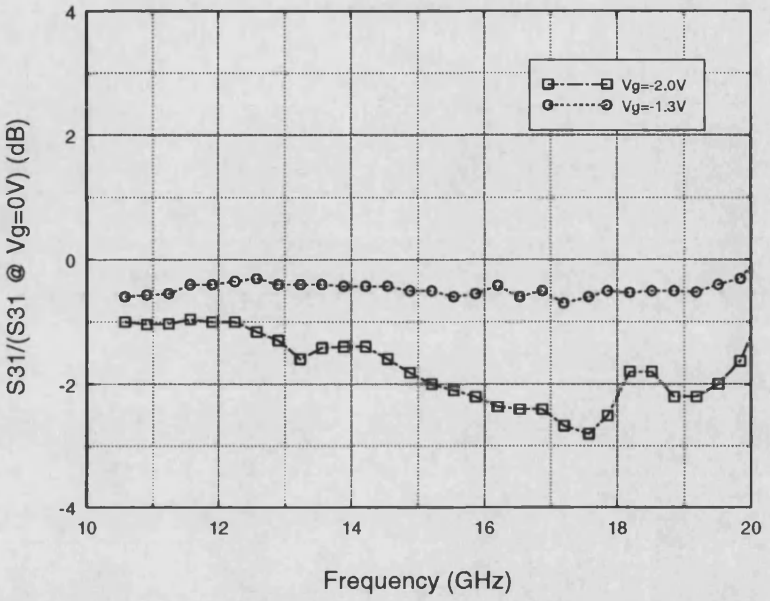

Figure 4.24: Variation in S_{31} for FET 1#11 mounted centrally

A similar magnitude of variation to that for FET 1#3 is obtained. The through transmission and backward coupling variation were also measured and are shown overleaf

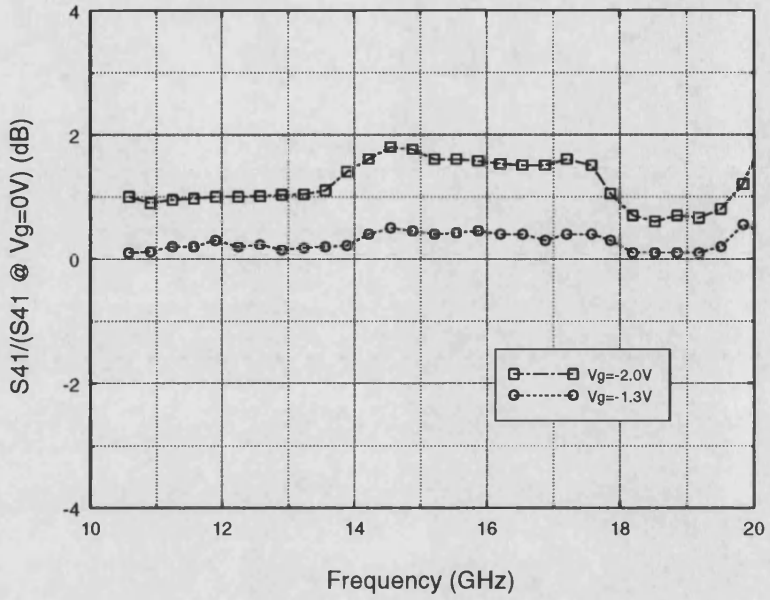

Figure 4.25: Variation in S_{41} for FET 1#11 mounted centrally

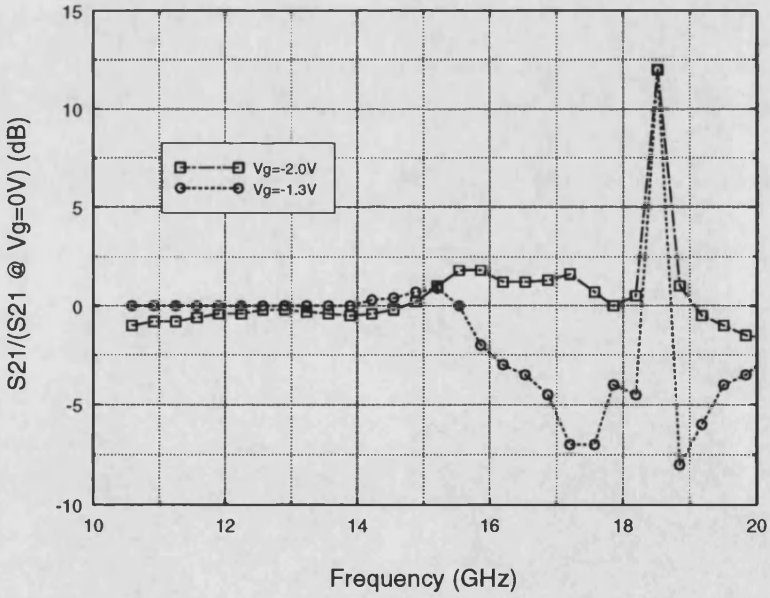

Figure 4.26: Variation in S_{21} for FET 1#11 mounted centrally

The general trends in these results is the same as those of FET 1#3, although the magnitude of the resonance in S_{21} is somewhat larger.

Finally lumped capacitors were added as previously to increase the through transmission, the results are shown below

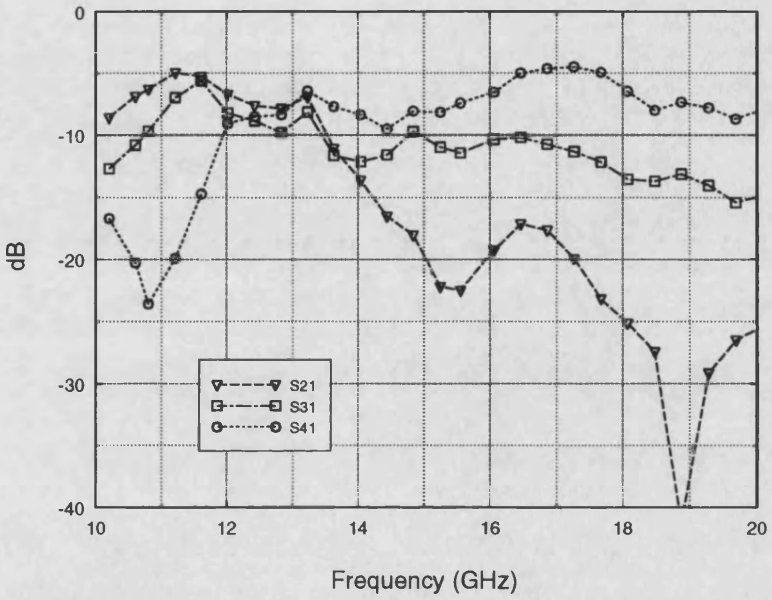

Figure 4.27: S-parameters for FET 1#11 with two added capacitors

Again, a dramatic improvement is obtained in the through transmission from 10-15dB to 4-8dB, the coupling is only slightly altered, however the backward coupling is substantially increased. As previously, the amount of variation in the forward coupling and through transmission has been reduced to $\simeq$1dB.

Conclusions

Voltage controlled directional coupling has been presented for two FET 1 type devices. Both exhibited similar trends, showing that the devices have reasonable repeatability. The effect of unsymmetrical mounting has been investigated and was found to have a marked effect on device performance. Attempts have been made to increase the level of the through transmission, a key parameter for a directional coupler, this has been achieved with the addition of lumped capacitors at the ends of the coupled region, however, this has led to a reduction in the amount of variation obtainable with gate bias.

These initial results have shown the large effect that external parasitics can have upon the measured performance of microwave devices. In the following section these parasitics will be reduced and very different performance will be obtained for the device, even so the results in this section are promising in themselves, with further work, such as integration of the lumped capacitors on chip and optimization of the capacitor values, useful voltage controlled directional couplers could be obtained.

4.3.4 Improved Test Fixture Results

In this section the level of the parasitics associated with the test fixture are reduced. The S-parameters of FET 1#11 were remeasured in the original test fixture (figure 4.14) with lumped capacitors removed, over the full 0.1GHz - 20GHz band.

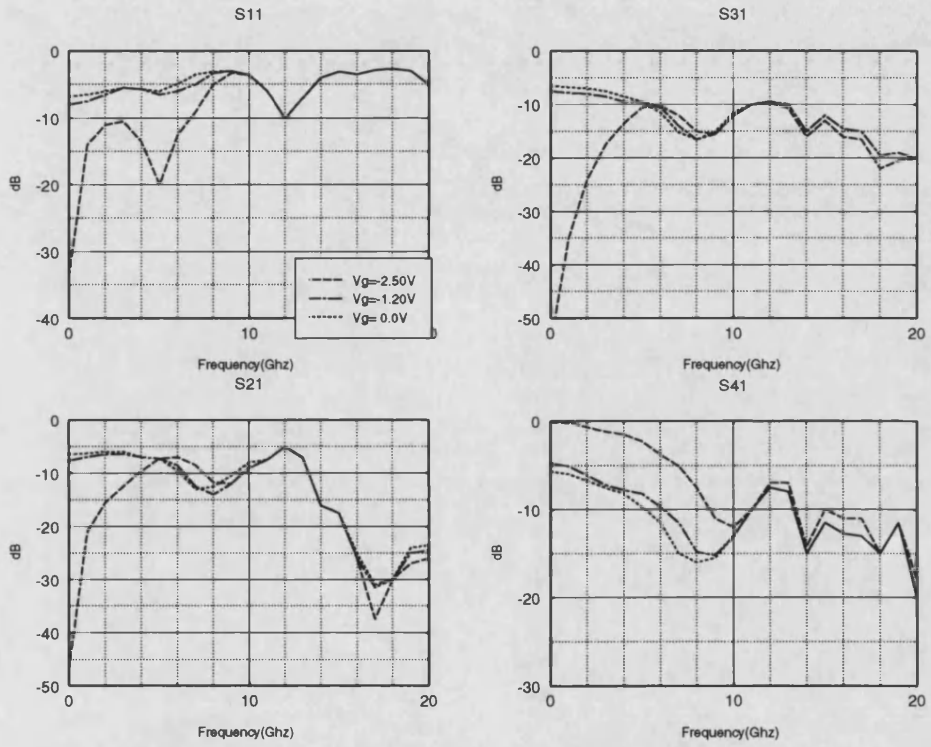

Figure 4.28: S-parameters for FET 1#11 in original test fixture

This format of results will be used throughout the rest of this work, that is : reflection coefficient, S_{11}, top left; forward transmission, S_{31}, top right; reverse transmission, S_{21}, bottom left; through transmission, S_{41}, bottom right.

The results are slightly different from the original measurements of figure 4.23 showing the sensitivity of these circuits at high frequencies to the mounting and unmounting of components, such as the lumped capacitors. These results show the low frequency behaviour of the wide FET : at zero bias, power incident on port 1 splits equally between ports 3 and 4, with slightly higher coupling to port 2, then as the gate bias increases, the channel

resistance increases and the source and drain lines become isolated. The forward and reverse transmission are seen to increase rapidly with frequency and $|S_{21}| > |S_{31}|$ up to 14GHz, this is the backward wave coupling that was anticipated for the device, similar to that obtained for two and three coupled lines [86]. When the channel resistance is high the reflection coefficient is reasonable, less than -10dB up to 6GHz and the through transmission is greater than -4dB. The directivity observed in the 0.1GHz - 14GHz region is very low $\simeq$ 4dB. As in the original measurements, forward wave coupling is observed above 14GHz.

The major parasitic element here is the inductance of the bond wires, this can be as much as 1nH per mm for 25μm diameter wire [103]. There are a number of ways to reduce the inductance : the diameter of the wire can be increased or a number of wires can be bonded in parallel. However, since the on chip bond pads are only 120μm square and the bonding is being done by hand with solder, either of these options would prove difficult. An alternative is to use gold tape, this can have a thickness of 25μm but can be very wide, thus reducing the inductance. The tape can be cut into a triangular shape and placed such that the base of the triangle is soldered to the microstrip line and the apex soldered to the on-chip bond pad. This produces a much lower inductance connection than a 25μm wire, from the measurements in chapter 3 and the modelling to be discussed later in this chapter the inductance value appears to be in the 0.2nH - 0.4nH range. Although lower in inductance, there is now a taper from 50Ω line width (2.4mm) to 120μm, this too will have parasitics associated with it, but these will be lower than for a single wire. The length of the taper is $\simeq$ 1mm and this is much less than a wavelength for most of the operating frequency, thus it will appear as a lumped inductance, with small fringing capacitance to ground.

FET 1#11 was rebonded with gold tape and S-parameters remeasured, they are shown below

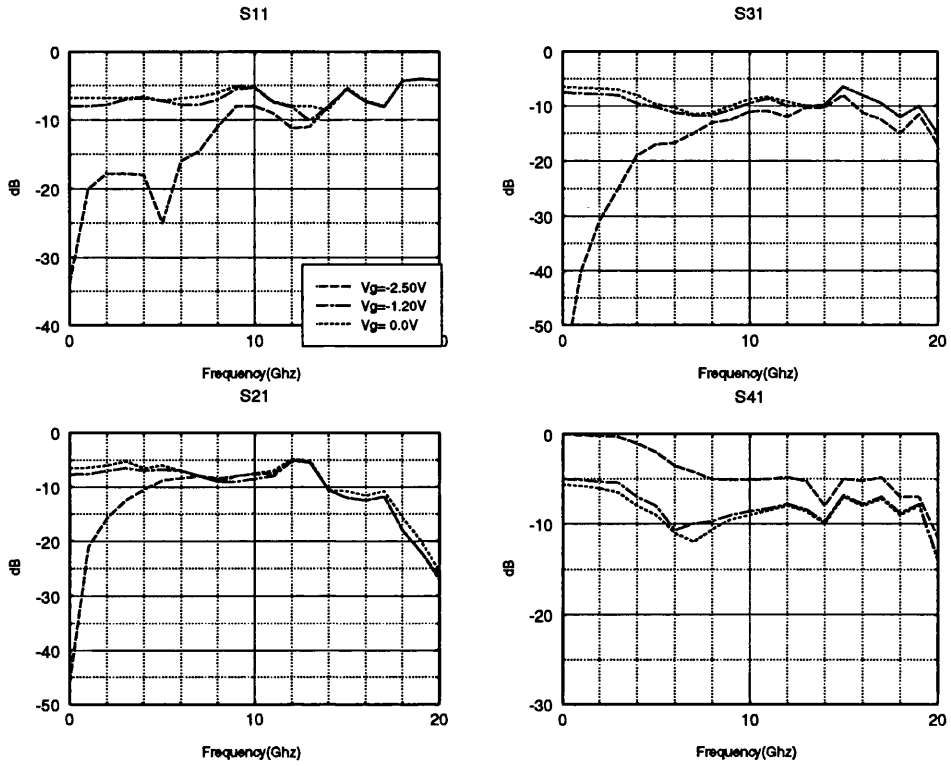

Figure 4.29: S-parameters for FET 1#11 with gold tape bonding

These results show dramatically different performance. The broad "peaking" around 6GHz has been removed and in the pinched-off state both the forward and backward coupling increase smoothly with frequency as is the case for passive coupled lines, below the quarter-wave frequency [86]. In the pinched-off state, backward coupling is again observed and the directivity is increased in this case to greater than 7dB up to 7GHz, the reflection coefficient is now less than -8dB up to 8.2GHz and the through transmission is greater than -8dB up to 19GHz. The high frequency region, greater than 14GHz is very different from the bond wire results as shown in figure 4.28, S_{21} is no longer at the low levels obtained previously, suggesting that the effects observed are due in part to the bond wires rather than purely the distributed coupling effects associated with the wide FET.

These results show the device has two regions of operation :-

(i) Near zero bias - as a voltage controlled power divider/combiner where power incident on port 1 splits equally between the three output ports, the magnitudes at the ports are controlled by the gate bias.

(ii) Near pinch-off - the device behaves as a set of coupled lines, which from 4GHz to 7GHz gives -10dB to -8dB of backward coupling, directivity greater than 7dB, reflection coefficient less than -14dB and through transmission greater than -5dB. The amount of voltage control at these levels is minimal.

The dual nature of the device could make it useful in applications where many functions are required to be integrated onto one chip.

Measured and Modelled Results

The inductive effect of the connections to the MMIC have been greatly reduced and the results are approaching those of the intrinsic device, these can now be compared with results from the basic model described in chapter 2. The equivalent circuit for the basic model is repeated here for completeness

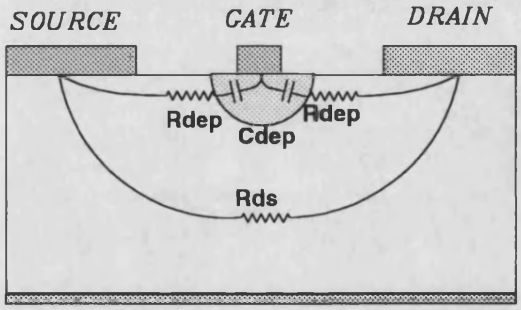

Figure 4.30: Basic equivalent circuit model for a wide FET

As discussed in chapter 2, the drain-source capacitance C_{ds} has been included in the inter-electrode capacitance, C_{31}. Firstly the inter-electrode capacitances must be calculated, in order to do this the geometry of the electrodes must be obtained. In the basic model zero thickness conductors are assumed, the MMIC layout diagram was used to obtain the electrode lengths and spacings. Length rather than width is used here to remain consistent with the use of the term "gate length".

The geometry of the FET is described below

Source length = 30μm

Drain length = 30μm

Gate length = 1.2μm

Drain to Gate spacing = 5μm

Source to Gate spacing = 5μm

Device width = 1500μm

The resistive network analogue [50] was then used to calculate the inter-electrode capacitances. The FET cross-section was discretized into a 1000 x 1000 grid and 90 of these nodes were placed symmetrically across the FET electrodes to obtained the reduced matrix. It is noted that the gate length is given here as 1.2μm rather than 0.7μm as discussed in the introduction. This was an attempt to maximize the number of nodes on the gate line. For gate lengths of less than 1.2μm only one node occurred on the strip, it was felt necessary to increase this to improve the accuracy of the capacitances. This results in 44 nodes across source and drain and 2 nodes across the gate. The speed of this method is dominated by the need to invert the 90 x 90 matrix, this was felt to be the best trade off for accuracy and speed. As with all finite difference methods, the problem of aligning node points with actual metal edges occurs, in fact with 44 nodes spaced across the source and drain, a node spacing of 0.68μm is obtained, this implies an effective gate width of 0.68μm much closer to the actual length, this was used as an initial estimate for the capacitances. Later an improved algorithm for the placement of nodes on the structure was developed such that 3 nodes were placed across the gate, giving an effective gate width of 1.39μm and results were found to be identical, a comparison of the results is shown in figure 4.31. This shows that the wide FET performance is dominated by the larger source and drain capacitances and the intrinsic FET elements.

Having obtained the inter-electrode capacitances, the values of the intrinsic FET elements must be determined. The pinched-off depletion capacitance was set using Ayasli's empirical expression [74] given previously as equation 2.47 and repeated here

$$C_{dep} = 60\frac{l_g}{a} \quad pF/m \tag{4.1}$$

Where l_g is the gate length in microns and a is the active layer depth in microns. The active layer depth was set to a=0.2μm, this is a typical figure for low noise GaAs MESFETs as given by Pengelly [75], the GMMT F14 process used to fabricate the devices is optimized for low noise performance [24]. Taking the gate length as 0.7μm, the pinched-off depletion capacitance is obtained as 210 pF/m. When the model was being developed, GMMT had no foundry data readily available for FETs used in this switching configuration (@ I_{ds}=0), thus comparisons for this calculated figure were difficult to find. However, in 1994 GMMT introduced a new process optimized for switching performance, and have produced modelled data for a 4 x 75μm FET, the pinched-off capacitance is given as 250pF/m [24], thus the estimate using Ayasli's expression was a reasonable approximation. A mid bias and zero bias capacitance were set as 500pF/m and 600pF/m respectively, these were chosen qualitatively to reflect the inverse square relationship of the voltage and capacitance in the simple Schottky barrier diode [104]. The other bias dependent parameter is the channel resistance R_{ds}, this was set to match the S-parameters measured at 0.1GHz, the values in distributed units were : 6mΩ.m (4Ω), 30mΩ.m (20Ω) and 90Ω.m (60KΩ), for the zero bias, mid bias and pinched-off cases (lumped values are shown in brackets). Finally the depletion resistance was set to 2.1mΩ.m (1.4Ω), a typical figure for this type of device [75].

The results for this model are shown below, two sets are shown, dashed lines for inter-electrode capacitances using 2 nodes on the gate line and marked points for 3 nodes on the gate line, it is seen that the results for the two cases are identical as discussed above.

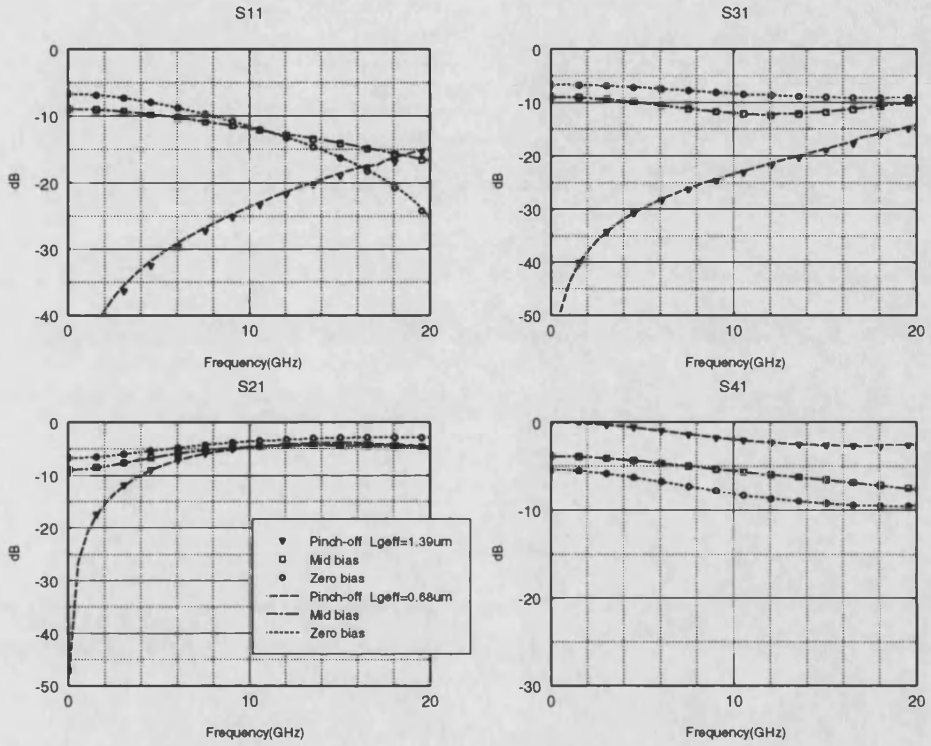

Figure 4.31: Simulated S-parameters using basic model with two different effective gate lengths

Comparing these results with those of figure 4.29 it is seen that all the basic trends are reproduced reasonably well for all three bias levels up to 10GHz. The absolute magnitudes are not reproduced exactly, however, this model does not include the effect of the tape bond connections and the differences between figures 4.28 and 4.29 illustrate the effect connection inductance can have on measured data. Thus, even though the level of the inductance has been reduced by the use of gold tape bond connections, it was felt inductive connections must be included in the model before any fitting of modelled to measured data could be carried out. This is introduced in the next section.

4.3.5 Model Improvements and Optimization

In the previous section it was shown that the basic model simulated the general trends of the wide FET reasonably well, more accurate fitting of the model was then required such that optimization of the geometry of the FET and other investigations using the model could be carried out. The major improvement required was the addition of the parasitic inductance of the tape bond connections, the methods employed for this have been discussed in section 2.5. The first method, using Mason's non-touching loop rule was used initially, but was found to be impractical for devices with more than four ports, since the wide FET is a six-port device a more practical method was sought. The second method discussed was then used, this was the transfer of the basic model wide FET S-parameters to a commercial circuit simulator, the simulator used was EEsof Academy^{TM}.

Thus, the basic model was used to produce the four-port S-parameters for the wide FET, the gate line being open circuit, thus even though the device is a six-port, at this point only four-port data is being used. The files containing this data are transferred from the mini-computer performing the simulation to the workstation platform running the circuit simulator. A four-port S-parameter data block is defined in the simulator for each of the three bias levels and lumped inductors can be added at each of the ports. The S-parameters shown in figure 4.31 were passed to the simulator and 0.3nH inductors were added to the ports, the results are shown overleaf compared with the measured data of figure 4.29

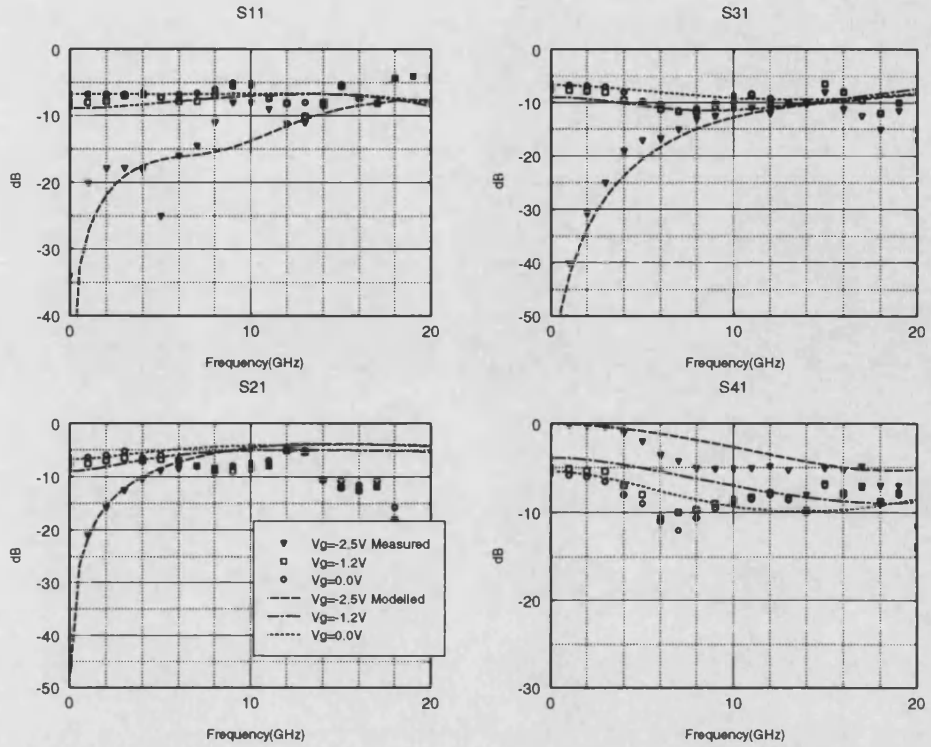

Figure 4.32: Comparison of measured with modelled S-parameters for basic model with connection inductances added, L=0.3nH

These results show that the basic model with added inductance simulates the wide FET well up to 10GHz apart from the "drop-out" in S_{41}, which may well be associated with the test fixture. The performance of the model above 10GHz is also quite good with the exception of the backward coupling, S_{21}, however, considering this is a quasi-TEM model, with all the inherent frequency limitations discussed in chapter 2, these results are very good.

Using the model, the effect of increasing the inductance of the connections was investigated. In order to see if the results in the original test fixture could be reproduced, the inductance was increased to 2.0nH, the results are shown below

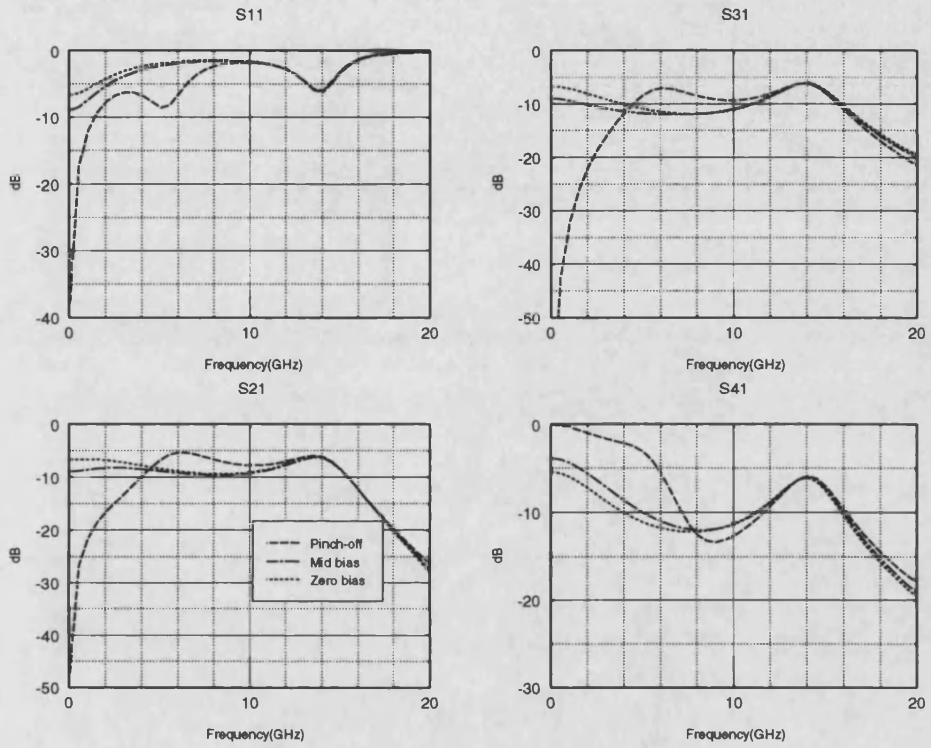

Figure 4.33: S-parameters for basic model with connection inductances added, L=2.0nH

Many of the features present in the measured results of figure 4.28 are reproduced, the magnitudes are not exact, but with fitting of data this could be improved.

These results show that the basic model with added connection inductances simulates the performance of the wide FET well with low inductance connections. It was felt that the model was sufficiently good at this stage to be used to investigate other FET electrode geometries with the aim of reducing the forward coupling, and hence increasing the directivity of the FET at pinch-off, the directivity being a key parameter for any directional coupler.

Wide FET Electrode Optimization

The basic model could now be used to investigate other electrode geometries, including overall device width, in order to optimize the directivity at pinch-off. The optimization procedure consisted of building up a data base of inter-electrode capacitances for a number of FET structures, simulating each of the structures with the same intrinsic FET model parameters and observing which gave the optimum directivity along with reasonable through transmission and reflection coefficient. The magnitude of the backward coupling was not a key parameter at this a stage, since this can vary greatly depending on the particular application.

A number of structures were investigated, a sample of the geometries simulated is given in the table below. These examples show the range of results obtained. In all cases the source and drain lengths are equal, so too are the source to gate spacing and drain to gate spacing, this was kept at 5.0μm and the device width was set at 1500μm

Device No.	Source Length (μm)	Gate Length (μm)
1	18	1.0
2	30	1.2
3	60	1.0
4	90	1.0
5	120	1.0

Table 4.10: Sample wide FET electrode geometries used for optimization

The table shows a broad range of source and drain lengths, gate lengths of 1.2μm for device No. 2 and 1.0μm for the other devices were chosen for ease of node placement in the calculation of inter-electrode capacitances and as has already been shown the S-parameter results are not sensitive to variation in the gate length.

The S-parameters for these structures were simulated using the basic model without connection inductances, this allowed all simulations to be performed on one system, with no transfer of data to a circuit simulator. The effect of the connection inductances would be to degrade

directivity and reflection coefficient as seen in the previous section, thus the optimization could be carried out on the intrinsic device since the inductances would have a similar effect on all devices. The S-parameters for the five devices are shown below, the prime interest was in the pinched-off directivity, thus only the pinched-off S-parameters are shown

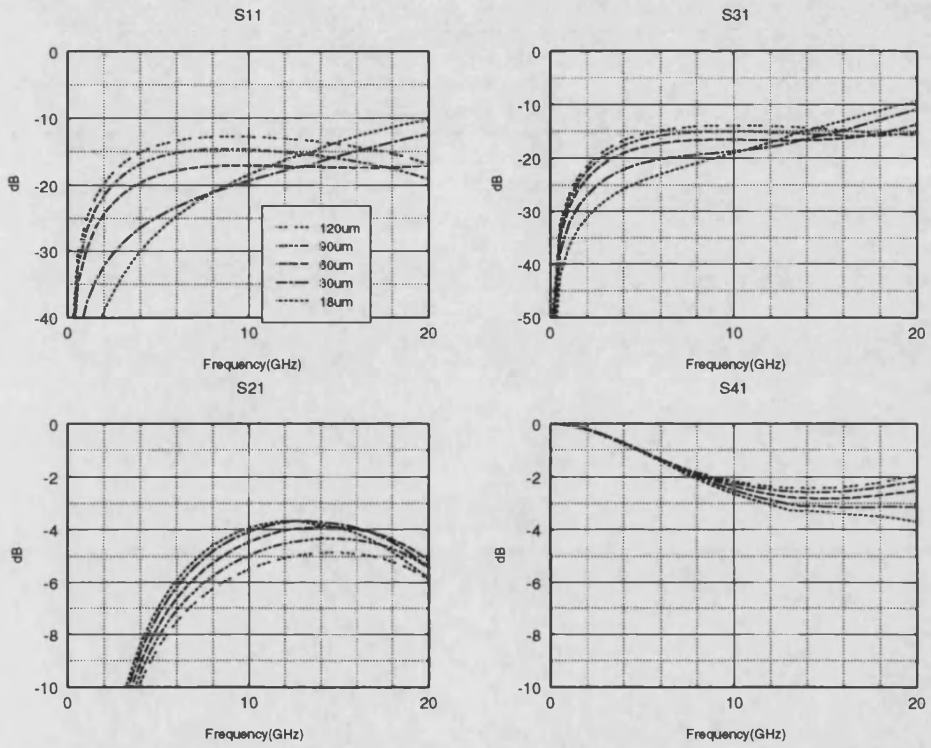

Figure 4.34: S-parameters at pinch-off for five wide FET structures with different source and drain lengths

There are a number of trends observed here, firstly, the backward coupling, S_{21} is greatest for the shortest source and drain length and decreases with increasing source and drain length, this trend also occurs in passive coupled lines and has been checked using EEsof Academy^{TM} for similar sized structures on GaAs. Secondly, the through transmission decreases with increasing electrode length, this trend is caused partly by the intrinsic resistive elements in the model, however, the major factor in this loss is the high level of forward coupling, backward coupling and reflection coefficient. Even in the case of a lossless ideal -3dB coupler the through transmission is -3dB, since power is splitting equally between the outputs. Thus, here, with backward coupling of -5dB for example it can be shown that the maximum through

transmission is -1.65dB, this does not include power reflected from port 1 or transmitted to port 3. Therefore, the trend observed in the through transmission can be thought of as resulting from the trends in the other S-parameters. Thirdly, the forward coupling, S_{31}, increases above 14GHz with decreasing electrode length, this will reduce the directivity, whilst below 14GHz the reverse is observed. The aim of this optimization was to produce high directivity, it was felt that it was more desirable to have good directivity in the high frequency region, above 14GHz, since it is often more difficult to obtain good directivities at higher frequencies for microstrip couplers as seen in the passive line results in this chapter. The choice thus seemed to be between the 60μm and the 90μm devices, further modelling to be shown later in this section, allowed one of these geometries to be chosen.

Gate Termination Optimization

The measured and modelled data presented in the first part of this chapter have referred to wide FET structures with open circuit connections on the gate line. However, the model developed allows the wide FET to be simulated with different gate terminations. Furthermore, having simulated the wide FET, different terminations can be connected to the existing wide FET structure and the predictions of the model can be checked against measured data. Initially, these terminations were envisaged as being mounted as lumped components on the the microstrip test fixture, improvements to this method will be detailed in this section. Initially the simulations were with no inductive connections, again to speed up total simulation time, they will be introduced later in the section.

Returning to the FET 1 structure with 30μm source and drain width, the gate terminations were reduced to 250Ω, the most interesting results were found at a slightly higher mid bias point than previously. The new mid bias point was at 90mΩ.m channel resistance, and since the reverse bias has increased, the depletion capacitance must decrease, this was set to 450pF/m. The results were resimulated for the open circuit case and are shown below, also shown are the S-parameters for the 250Ω terminated gate line.

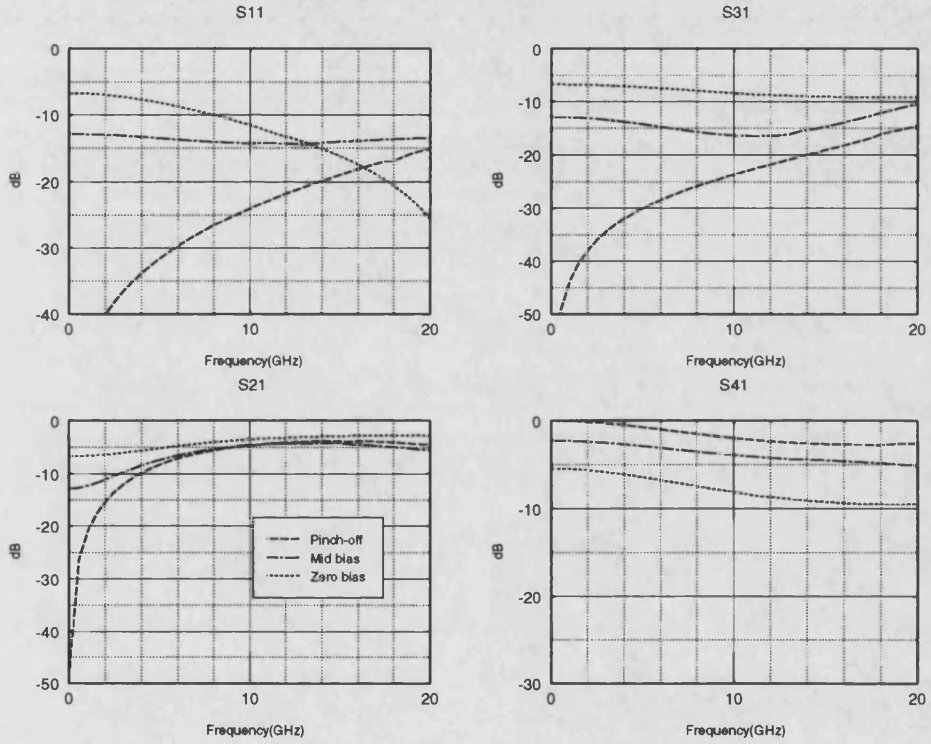

Figure 4.35: S-parameters 30μm device with open circuit gate line

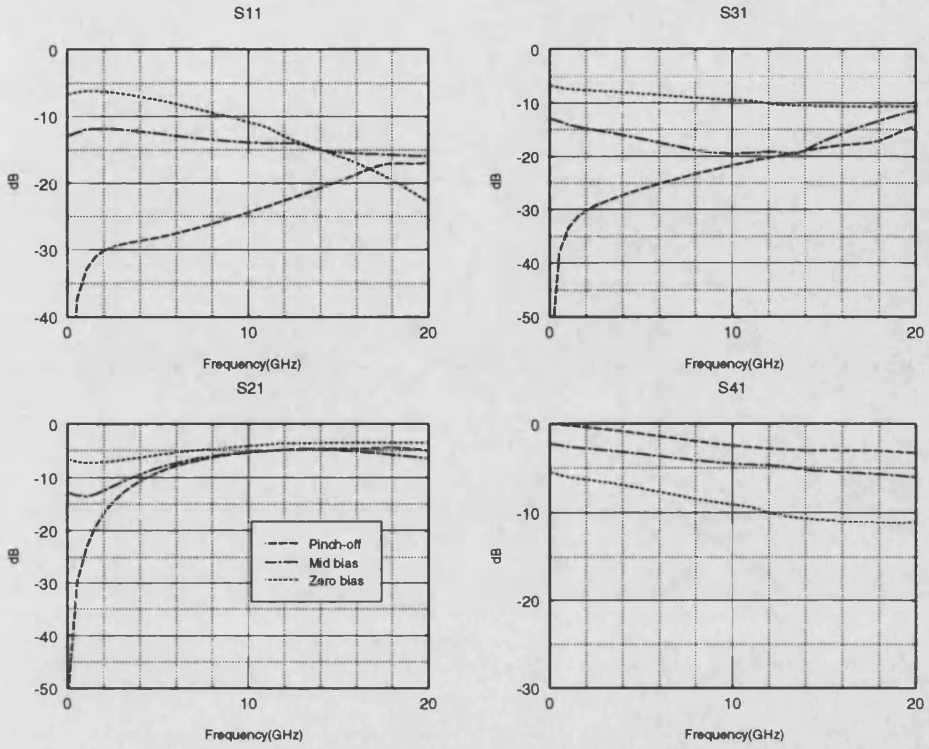

Figure 4.36: S-parameters 30μm device with 250Ω terminated gate line

It is noted that for the mid bias case that with 250Ω terminations the forward coupling is 3dB-4dB less than for the open circuit case, with little change in the backward coupling, thus the directivity has increased. If the terminations are further reduced to 50Ω, further interesting results were obtained, shown in figure 4.37

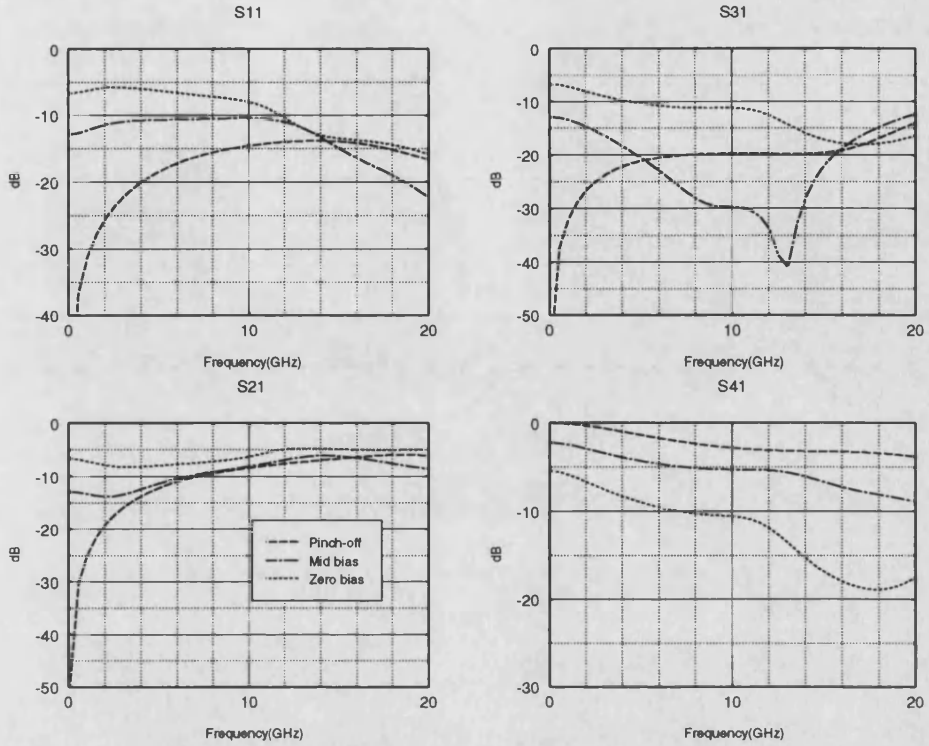

Figure 4.37: S-parameters 30μm device with 50Ω terminated gate line

These results show that the mid bias forward coupling now has a resonance around 13GHz, giving < -35dB forward coupling from 12GHz - 13.5GHz, the backward coupling is $\simeq$-7dB, this gives 28dB directivity, which even though over a small bandwidth is extremely high for a monolithic microstrip coupler. If 20dB directivity is taken as the specification then the bandwidth is from 8.5GHz - 14GHz, this is very good performance and compares well with commercially available microstrip coupler, for example MA-COM quote a 10dB coupler with a bandwidth of 7.0GHz-12.4GHz with a directivity of 20dB [101]. The commercial coupler has a backward coupling flatness with frequency of $\pm$1dB, the wide FET has $\pm$1.3dB, again, reasonably good.

Having used the basic model to predict this improved performance, the electrode optimization procedure was repeated with 50Ω terminations. The results are shown below

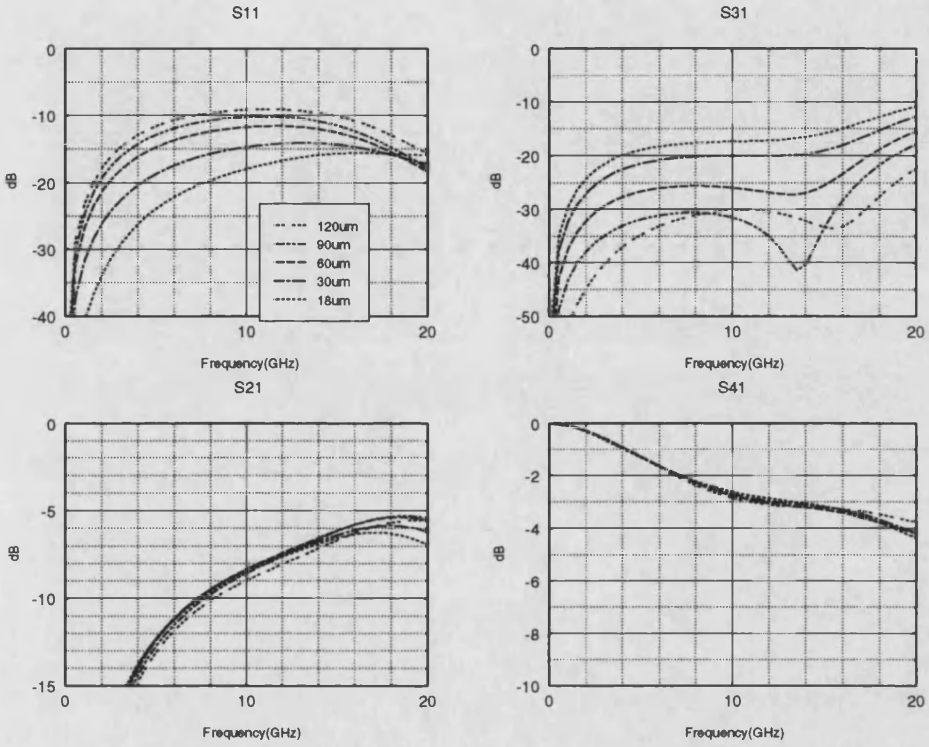

Figure 4.38: S-parameters at pinch-off for five wide FET structures with different source and drain lengths and 50Ω terminated gate line

These results show the 90μm device gave better performance than the 60μm device across the whole band. The 120μm device was better at higher frequencies, but it was felt that the improvement in the 90μm device over the 120μm device in the 10GHz to 14GHz range warranted choosing the 90μm device.

The model was then used to investigate the effect of device width on its performance. The 90μm device was simulated at 1000μm and 2000μm to show the trends in performance around the original width of 1500μm. These results are shown below

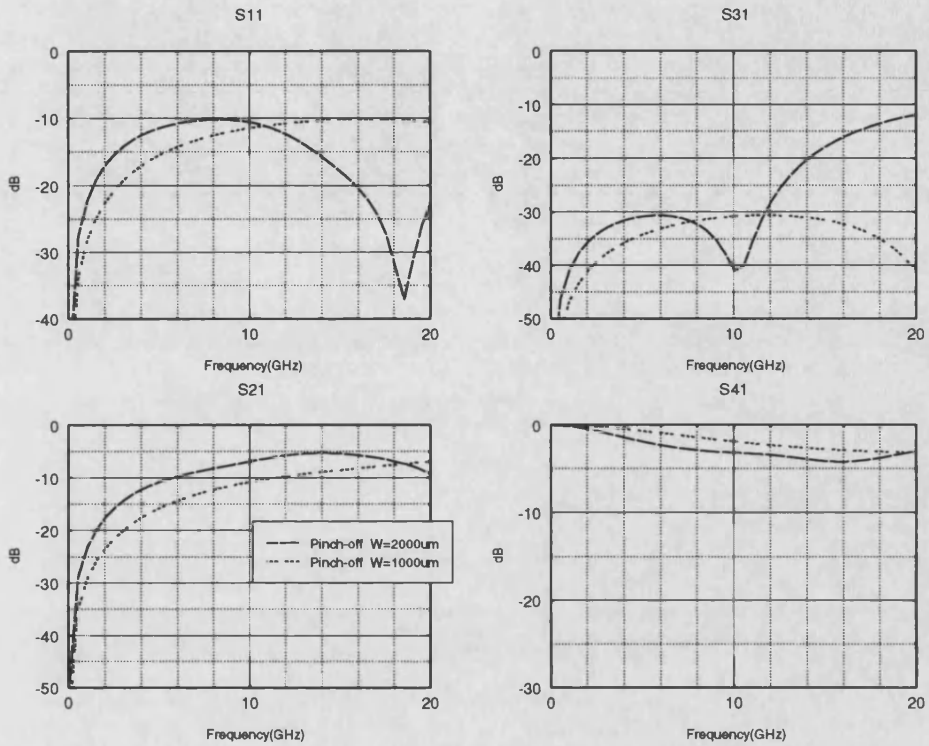

Figure 4.39: S-parameters at pinch-off for 90μm device with two different widths

The zero bias and mid bias S-parameters were reasonably insensitive to device width and thus are not shown to aid the clarity of the results. It is seen that as for passive lines, as the device width increases the frequency of maximum backward coupling, S_{21} decreases. For the wider device the forward coupling, S_{31}, increases at high frequencies, resulting in reduced directivity. As would be expected, the narrower device also results in higher through transmission. Thus a device width of $\simeq$1300μm was chosen, this should result in good high frequency directivity, with reasonable backward coupling and through transmission. At this stage the improvements in mid bias performance over pinched-off performance had not been fully validated by comparison with measured data and thus it was decided to continue with the 90μm device for fabrication, the results are presented and discussed in detail in chapter 5.

It must be remembered that this model contained no inductive connections, the effect of these was added for comparison with measured data, inductances of 0.3nH were added to the four ports, the gate was terminated with 50Ω resistors in series with 1.8nH inductors. This inductance is made up of 0.3nH for the tape bond and 1.5nH for the resistor - through substrate wire bond combination. The level of this inductance was determined by mounting the resistor in a 50Ω transmission line and measuring it in both grounded and in-series configurations, these measurements are discussed in chapter 3. The modelled wide FET S-parameters are shown below

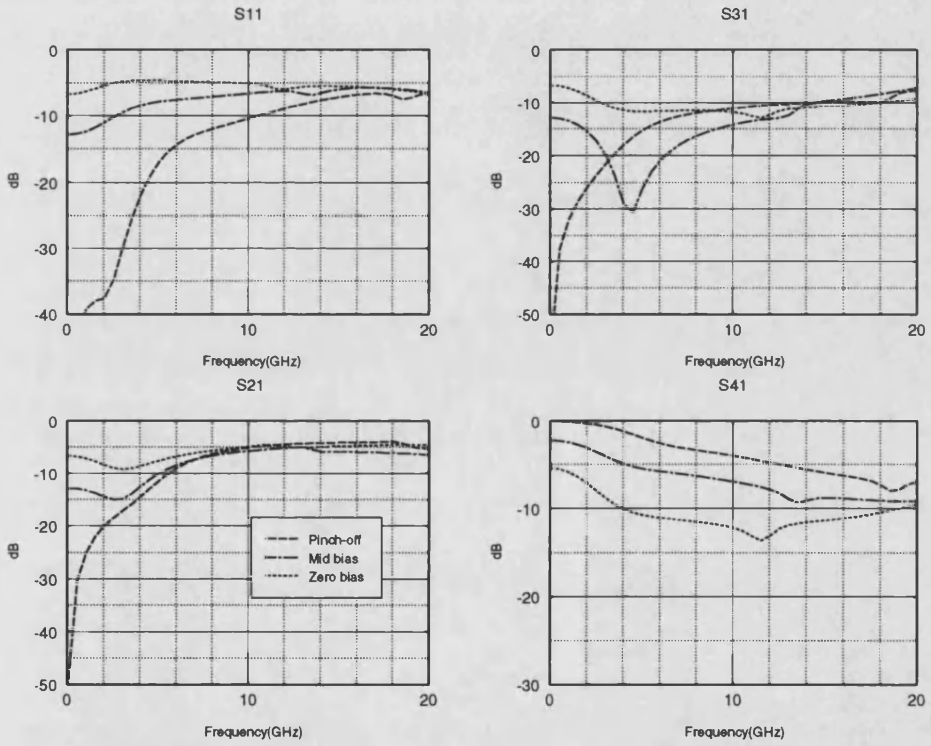

Figure 4.40: Modelled S-parameters for 30μm device with 50Ω terminated gate line and inductive connections

The figure shows the large effect of the inductive connections. The forward coupling is much larger in both the pinched-off and the mid bias states. The resonance has shifted to a much lower frequency and high directivity is obtained over a much smaller bandwidth. This degradation in performance was anticipated, since port 2 is terminated in a non-ideal 50Ω and the reflection from this port will add directly to the forward coupling signal at port 3 as discussed in chapter 3. This model is representative of the measurement situation and shows that even with tape bond connections in place, the resonant behaviour of the forward coupling should be observed.

Having used the model to predict this interesting mode of operation for the wide FET, 50Ω terminations were added to FET 1#11 in order to check the model prediction. Chip resistors were epoxied to the microstrip substrate, they were taped bonded to either end of the gate line and grounded with a through substrate wire bond. The major problem with this configuration was that the resistors provided a d.c. path to ground for the gate bias, thus high currents would flow on the gate line. To overcome this problem, the gate bias was only applied for short periods, later microwave d.c. blocking capacitors were obtained, results using these are shown in the next section. The results for FET 1#11 are shown below

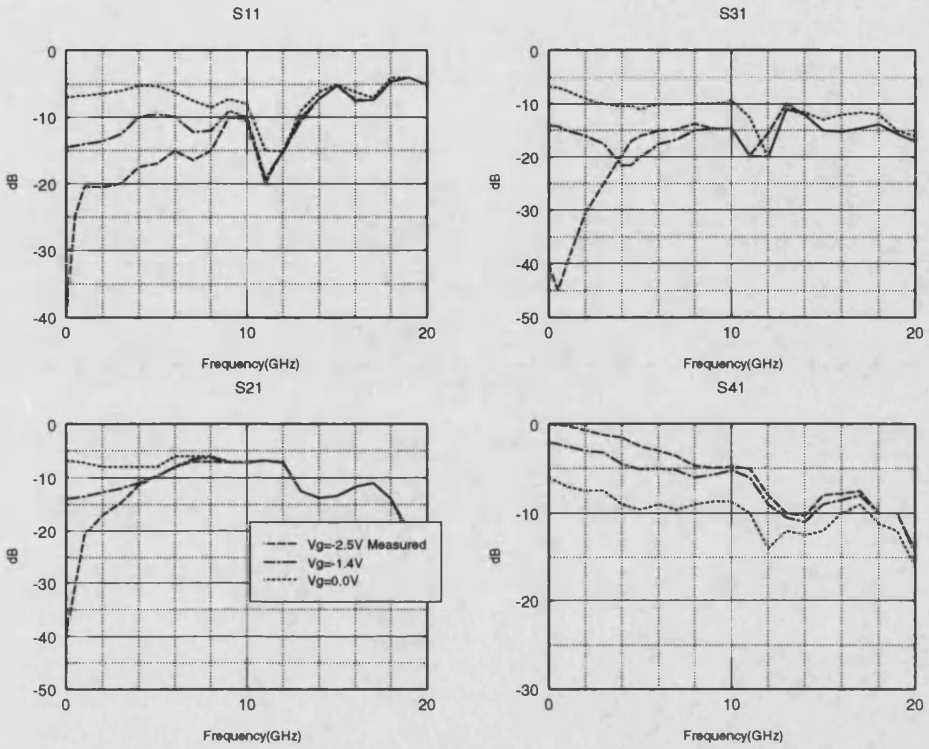

Figure 4.41: S-parameters for FET 1#11 with 50Ω terminated gate line

Comparing figures 4.40 and 4.41 it is seen that a resonance is observed at approximately the predicted frequency, but is of much lower Q, the pinched-off forward coupling is also lower than predicted. The other S-parameters agree reasonably well. If these results are compared with the open circuit gate line results of figure 4.32, it is observed that the directivity has not been increased, in fact in the pinched-off state it is slightly less. The bias level of the mid bias point is also noted as being different, however, the resonance observed in the 50Ω terminated case was not observed at any bias level in the open circuited case.

Although the level of performance predicted by the model has not been attained, a resonant behaviour has been observed. The 50Ω terminations used are far from ideal and possess large parasitic inductances, it was felt that if they could be reduced, improved performance and agreement with the model could be obtained. The next section discusses the methods used to reduce the gate termination parasitics.

4.3.6 Further Test Fixture and Model Improvements

Introduction

It has been seen that the addition of 50Ω terminations to the gate line of a wide FET produces a resonant behaviour in the forward coupling of the device. In addition to this however, from the definition of S-parameters [53, 54], which require all ports to be terminated in a finite impedance, it is seen that with 50Ω terminations on the gate line, the wide FET is configured for the first time as a true six-port with a system impedance of 50Ω. Neglecting momentarily the parasitic inductances of the terminations, the four S-parameters shown in figure 4.41 are in fact four of the eight S-parameters required to characterize a symmetrical six-port.

These ideas led to the conclusion that the gate line need not be terminated on the microstrip substrate with poor quality chip resistors, but could be terminated by 50Ω microstrip transmission lines and external, high precision, coaxial 50Ω loads, in the same manner as the four ports of the source and drain lines had been. This would not only reduce the parasitics of the gate terminations to a minimum and hence approach the high directivities predicted by the model, but also allow full six-port characterization of the wide FET, giving four more S-parameters which would aid in the fitting of measured to modelled data.

Test Fixture Improvements

In order to implement these ideas a new microstrip mounting circuit was required. To further reduce connection parasitics a high dielectric constant substrate was used, with ϵ_r=10.5, and height = 0.635mm, this would reduce the 50Ω line width from 2.4mm to 0.59mm, resulting in a much smoother transition from microstrip to the 120μm MMIC bond pad. The reduction in line width also increased the spacing of the incoming microstrip lines which would minimize any coupling effects between these lines. The circuit layout used is shown overleaf

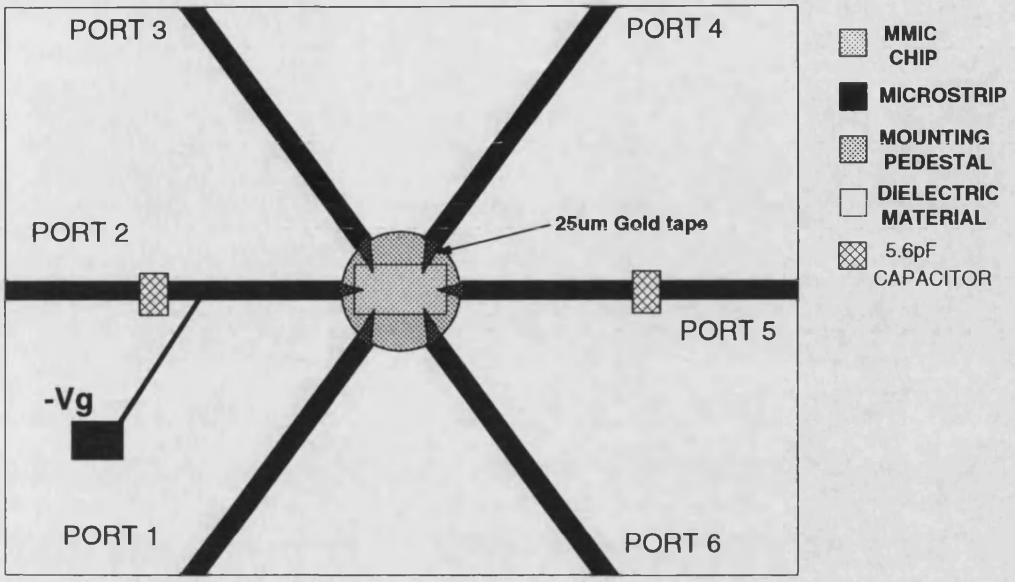

Figure 4.42: Six-port Wide FET test fixture

The figure shows the six microstrip lines connected to each of the six ports of the wide FET. Since the wide FET is configured as a six-port the port numbering scheme has been changed as shown above. Forward coupling from source to drain is now S_{41} and backward coupling from source to drain is S_{31}. Another important feature is the inclusion of d.c. blocking capacitors, these are single layer high performance ceramic capacitors, initially the only value available was 5.6pF, later this was increased to 56pF. This allows d.c. to be applied to the gate without drawing large currents. The performance of these capacitors is discussed in detail in chapter 3. The gate bias was applied through a high impedance transmission line.

FET 1#14 was mounted in this configuration and the six-port S-parameters were measured, the source - drain associated S-parameters are shown in figure 4.43

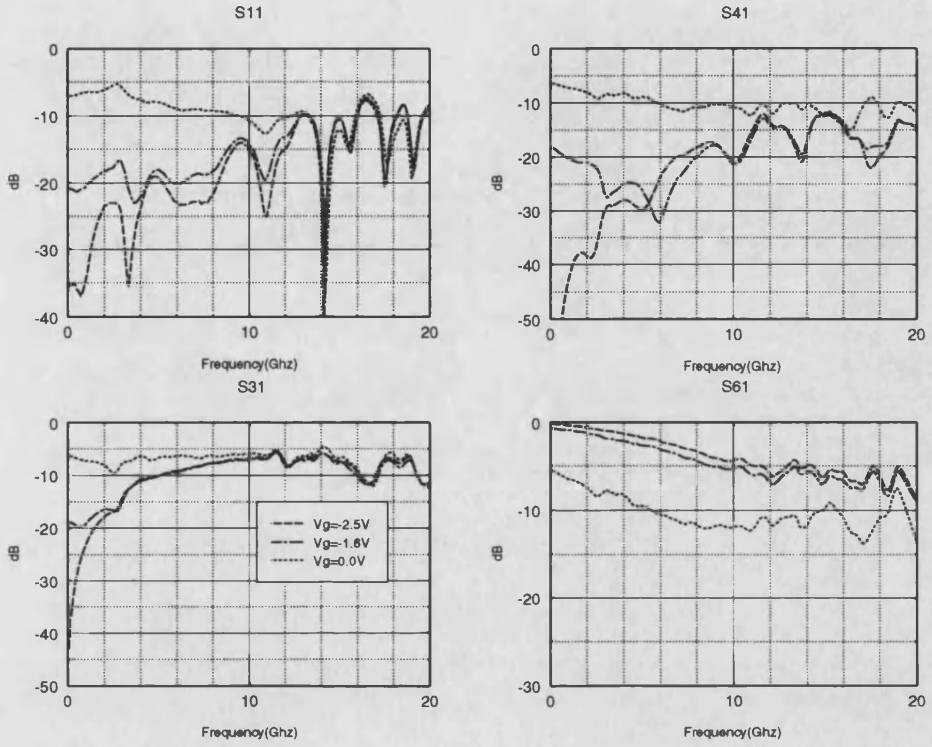

Figure 4.43: Source - drain S-parameter for FET 1#14

Comparing these results with those of figure 4.41 it is seen that the forward coupling, S_{41} is much lower in both the mid bias and pinched-off states, resulting in higher directivity as predicted. The resonant behaviour of the mid bias state is again observed and is 9dB lower than the pinched-off state at 5.9GHz. The high frequency behaviour is also very different, the fall off above 14GHz in the backward coupling and through transmission observed in figure 4.41 is no longer present in the new test fixture results. All these improvements are a result of the lower level of parasitics associated with the new test fixture. Having achieved this improved performance, the detailed characteristics of the wide FET were analysed over the 4.0GHz - 10.75GHz bandwidth where the device has its optimum performance as a directional coupler. The backward coupling and directivity are plotted overleaf for this reduced band

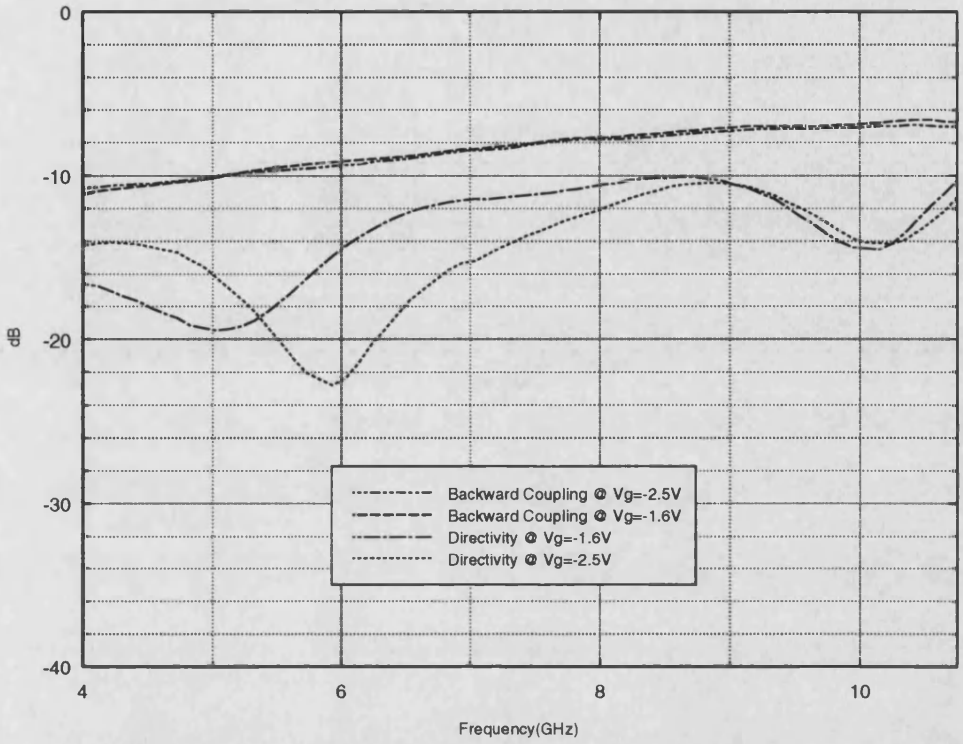

Figure 4.44: Coupling and directivity for FET 1#14

Across this band the coupler has a nominal coupling level of -8.9dB and a coupling flatness of ±2.2dB. The directivity is always greater than 10dB (plotted as a negative quantity for convenience), but moreover, the level of the directivity is tunable. It is well known [105] that in reflectometer measurement systems that the directivity of the measurement coupler defines the accuracy with which a return loss can be measured. Thus the high directivity band could be tuned to the band of interest and improved accuracy obtained. The tunable directivity would also allow rigorous directivity specifications to be met with high yields, by using post-fabrication tuning, a luxury not often available to the MMIC designer.

The other parameters of the coupler, through transmission and reflection coefficient are shown below

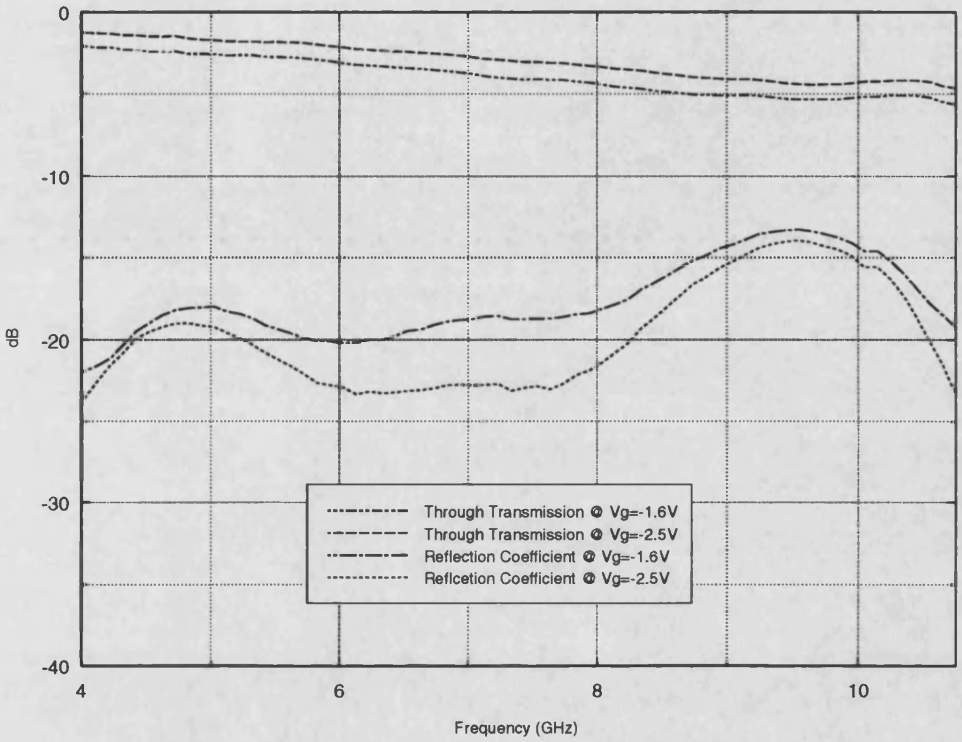

Figure 4.45: Through transmission and reflection coefficient for FET 1#14

It is seen that the reflection coefficient is always less than -13dB, a reasonable level considering the presence of the tape bond inductances. The through transmission is always greater than -5.6dB, part of this loss is due to the high level of backward coupling, for this wide FET with nominal coupling of -8.9dB a through transmission of -1.2dB occurs due to the high coupling level. The test fixture will also introduce loss in transmission lines and tape bonds, however the losses associated with this test configuration are near the minimum possible and any further reduction would require alternative techniques i.e on-chip probing, as discussed in chapter 3. Any remaining loss will be associated with the wide FET structure, and this can be investigated using the model that has been developed.

The new test fixture allowed the measurement of the S-parameters associated with the gate line, they are shown below in the same format as the source-drain S-parameters, note that the mid bias point is different from that for the source - drain S-parameters, later in the section all S-parameters are measured at equal bias points

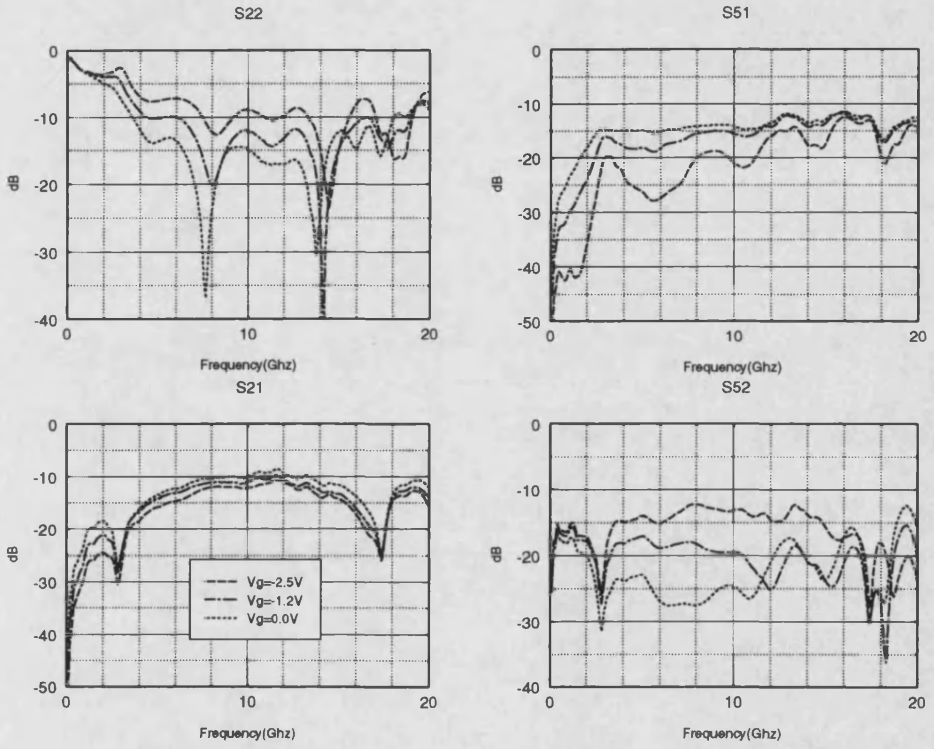

Figure 4.46: Gate S-parameters for FET 1#14

There are a number of features to note here, firstly at pinch-off backward coupling is observed from 4GHz - 14GHz at a lower level than for source and drain lines, as might be expected since the gate line is very short $\simeq 1\mu$m. Secondly, there are two regions of resonance, one around 3GHz, the other around 17GHz, which effect all the S-parameters. Thirdly, the level of the through transmission is generally much lower than for the source or drain lines. Fourthly, the level of the through transmission at 0.1GHz is masked by the presence of the 5.6pF d.c. block.

The main feature of these results is the sharp resonances, it was felt that since they were present at all bias levels and effected all S-parameters, they were most likely caused by the

test fixture rather than the wide FET itself. Using the circuit simulator, d.c. blocking capacitors and high impedance transmission line chokes were added to the basic model, and it was found that the resonances were indeed associated with the bias circuits. To remove these resonant effects either higher value capacitors, inductors, or both were required, these problems have been discussed in chapter 3, an increased inductance solution will be discussed later in this section and higher capacitances will be used in chapter 5. As an interim measure to obtain the gate S-parameters, the internal bias tees of the HP8510 VNA were used to apply bias to the gate line. This removes the need for any d.c. blocking capacitors or chokes, however, this also limits the bias dependent measurements to those S-parameters associated with the gate line. FET 1#7 was mounted in this test configuration and the gate S-parameters measured and are shown in figure 4.47

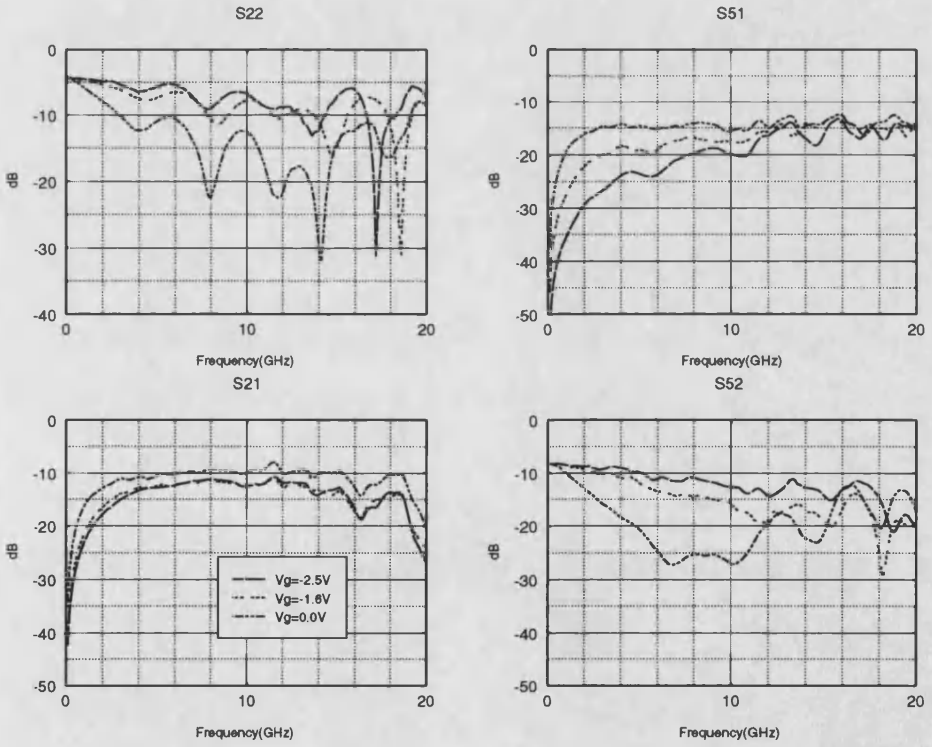

Figure 4.47: Gate S-parameters for FET 1#7 using HP8510 internal bias tees

The results show that the resonances have now been removed and backward coupling is observed from very low frequency up to 12GHz in a similar manner to the source and drain lines. Variable directivity is again observed, however, at a much lower level, than for the

source - drain lines and with no resonant behaviour. The through transmission, S_{52}, is still much lower than for the source - drain lines, and level at 0.1GHz is $\simeq$-8dB, implying a high d.c. loss mechanism.

For modelling purposes it is important that the gate S-parameters are measured at the same bias points as the source - drain S-parameters, this could only be achieved using on-substrate bias circuits, coaxial bias tees which could be moved from port to port as required would also provide this but were not available. Thus the performance of the on-substrate bias circuits had to be improved, as discussed above the values of inductance and capacitance used needed to be increased, higher value capacitors were not readily available, however, high value inductors could be obtained by using wire wound coils. These could be manufactured in-house using enamel coated wire. The design of these coils is discussed in chapter 3. After some experimentation reasonable performance coils were obtained, thus the high impedance transmission line choke was replaced with the choke coil, this enabling full six-port characterization.

The mounting circuit for FET 1#14 was modified to take the choke coil and the S-parameters remeasured and are shown in figures 4.48 and 4.49

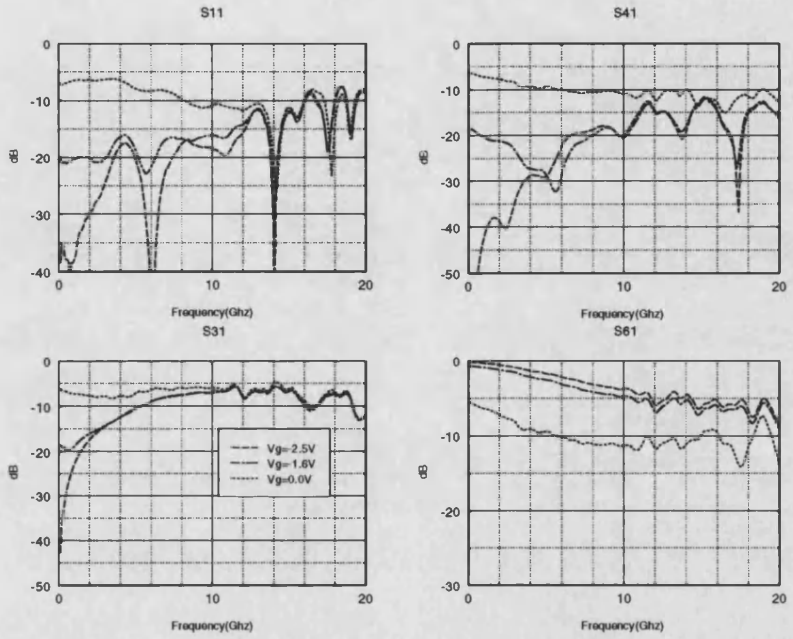

Figure 4.48: Source - drain S-parameters for FET 1#14 with added choke coil

Comparing the source - drain S-parameters to those of figure 4.43 they are seen to be very similar, showing that the gate bias circuit did not have a major effect on these parameters.

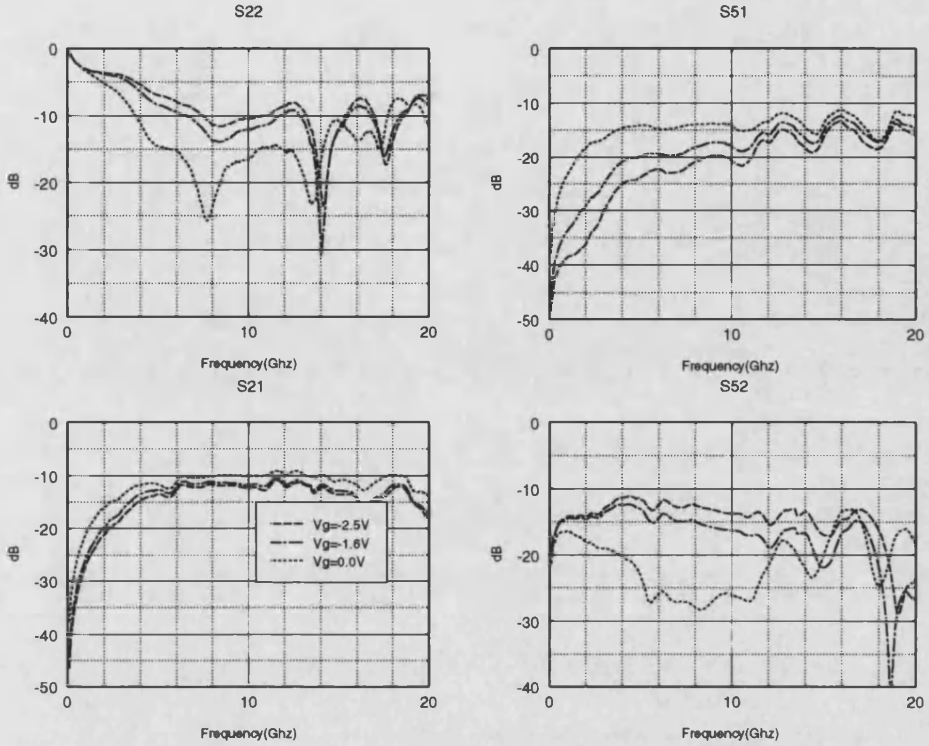

Figure 4.49: Gate S-parameters for FET 1#14 with added choke coil

The gate S-parameters are, however, very different from those of figure 4.46 and are much closer to those of figure 4.47 where no bias circuits were used. The very low frequency region is still affected by the low value of capacitance of the d.c. blocks. Thus the addition of choke coils to the bias circuit has been shown to reduce the effect of bias circuitry on measured S-parameters, the inclusion of high value capacitors in the next chapter will produce high performance broadband bias circuits.

Thus in the new test fixture of figure 4.42 much improved performance for the wide FET as voltage controlled directional coupler has been obtained. Tunable directivity has been shown over a wide band along with reasonable coupling flatness, reflection coefficient and through transmission. The model that has been developed will now be fitted to this latest measured data, firstly the newly obtained S-parameters will be investigated.

Modelling of Wide FET Six Port S-parameters

Having removed bias circuit effects from the measured gate S-parameter data, this could now be compared with results from the basic model, the S-parameters are shown here with connection inductances L_c=0.3nH on all ports, depletion capacitance C_{dep}=600, 450, 210pF/m at the three bias levels, channel resistance, R_{ds}=6mΩ.m, 0.24Ω.m, 90Ω.m and R_{dep}=2.1Ω.m

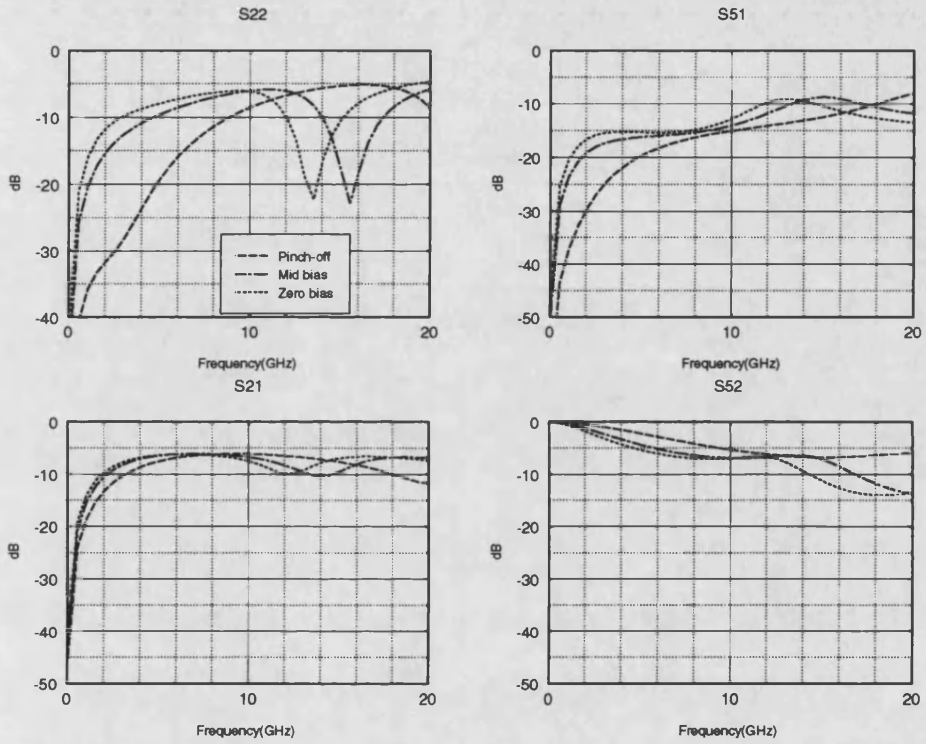

Figure 4.50: Modelled gate S-parameters for FET 1 type device

These results show major differences from the measured data, especially at very low frequencies, where for S_{22} and S_{52} there is no agreement. The basic model, while being able to simulate the source-drain S-parameters reasonable well, was obviously missing a key parameters associated with the gate S-parameters. It became apparent that a large series resistance on the gate line could account for the effects observed in the measured data. Since the gate line was very wide $\simeq$1500μm and has a very small cross-section, a high level of resistance was very possible. To confirm this, simple d.c. resistance measurements were carried out on the gate line, the resistance was found to be 155.5Ω. Using the well known formula for

the S-parameters of a series impedance [53] this series resistance was converted to equivalent S-parameter, and gives S_{52}=-8.15dB, this compares very well with the measured value of S_{52}=-8.14dB at 0.1GHz. This resistive effect was included in the model by introducing a real part to the complex distributed series impedance matrix of the FET electrodes. The distributed resistance in Ω/m for a 1.5mm wide device is 103.7kΩ/m, the drain and source electrode resistances were also measured and found to be 1.1Ω, equivalent to 733Ω/m. The model was resimulated with the same values as in figure 4.50, but with added electrode resistances, the results are shown below

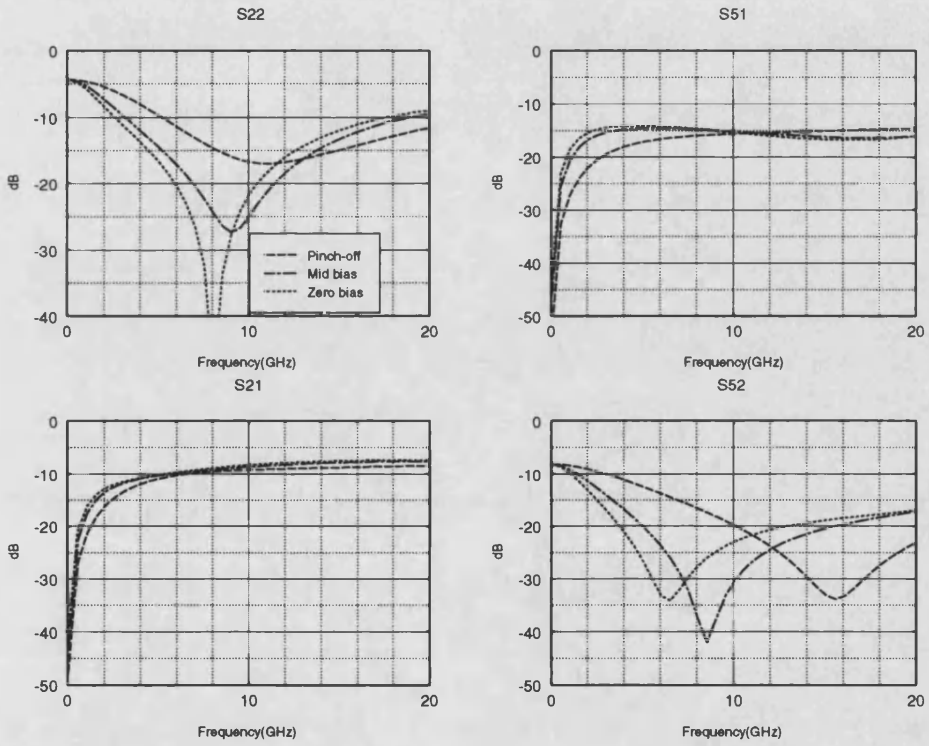

Figure 4.51: Modelled gate S-parameters for FET 1 type device including electrode resistances

It is seen that good low frequency agreement is now being obtained. Also, for the zero bias case, reasonable agreement is obtained across the whole bandwidth. However, for the mid bias and pinched-off states, while the general trends are correct, the absolute magnitudes are not in good agreement.

The effect of the electrode resistances on the source - drain S-parameters must also be assessed. In figure 4.40 the S-parameters are shown for 0.3nH inductances on the source and drain ports and 2.0nH on the gate ports, in the new test fixture 0.3nH is placed on all ports, the basic model S-parameters with no electrode resistances are shown below and overleaf with added electrode resistances

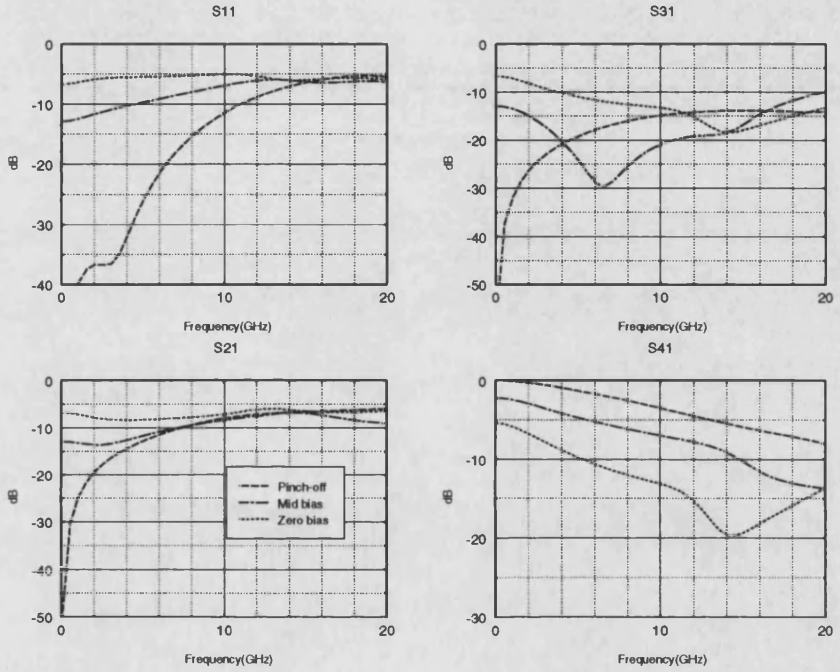

Figure 4.52: Modelled source - drain S-parameters for FET 1 device with L_c=0.3nH on all ports

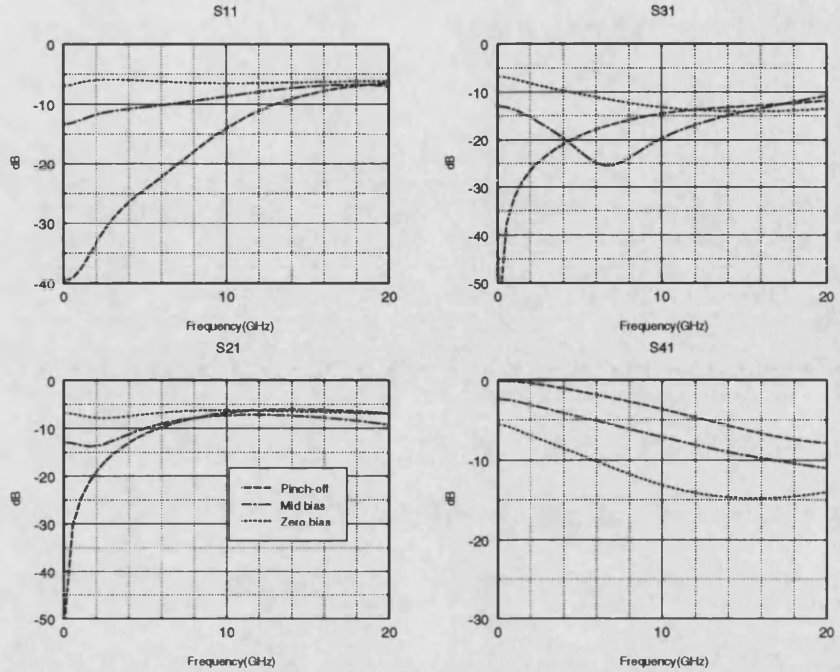

Figure 4.53: Modelled source - drain S-parameters for FET 1 device with L_c=0.3nH on all ports and added electrode resistances

It is seen that the S-parameters above 12GHz with added electrode resistances do not possess the resonant behaviour of the basic model S-parameters, and comparing to the measured data of figure 4.43 this would seem more representative of the observed trends.

A further enhancement to the model must also be noted, the basic electrode geometry of the FET had remained unchanged up to this point, that is :

Source length = 30μm

Drain length = 30μm

Gate length = 1.2μm

Drain to Gate spacing = 5μm

Source to Gate spacing = 5μm

Device width = 1500μm

Following technical discussions with Eurochip, it became apparent that even though the MMIC layout defined a 30μm length for the source and drain electrodes, the actual length, due to the mesa effect of the etching process, was increased by 2μm per side, giving a new length of 34μm. Allied to this was the fact that beneath, the third metal layer (M3) was a much thinner seed layer metal (M1), used to improve the contact between the GaAs and the M3 layer. The M1 metal extended beyond the M3 metal by 2μm per side, resulting in a total metal width of 38μm. These discussions resulted in a new FET 1 structure :

Source length = 38μm

Drain length = 38μm

Gate length = 1.0μm

Drain to Gate spacing = 2.3μm

Source to Gate spacing = 2.3μm

Device width = 1500μm

The effects of this change in structure are shown below, using the same model data as in the last section, but with the two different structures

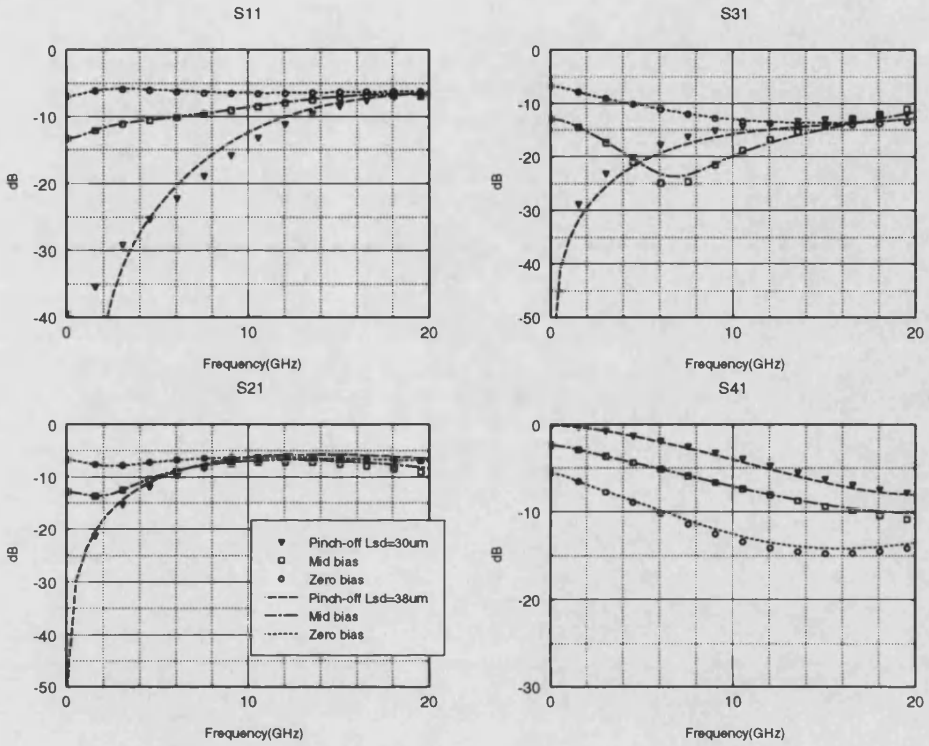

Figure 4.54: Comparison of wide FET models with 30μm and 38μm source and drain lengths

Only small changes are observed and all the previous trends including the resonant behaviour of the mid bias forward coupling are present. Similar results are also obtained for the gate S-parameters.

At this point it was felt that a good model for the device had been developed which reproduced all the observed trends in both source - drain and gate S-parameters and that optimization of the model parameters could now be used to obtain good agreement between measured and modelled data.

Fitting of Modelled to Measured Data

In order to carry out this procedure efficiently the effect of the tape bond connections had to be included in the intrinsic model, this would remove the need to transfer S-parameters to a circuit simulator and facilitate rapid processing of the complete model. This was implemented as described in section 2.5 by the multiport connection method, this enabled the complete model to be simulated at 41 frequency points in approximately 5 seconds on a series 9000 HP minicomputer. Thus a large number of iterations could be performed very quickly, and since the fitting procedure was a manual one this was essential.

The fitting procedure was now undertaken, this was to be a manual procedure, whereby the model simulations were compared to the measured data, and the relationship between modelled S-parameters and the model parameters was obtained by performing a spread of simulations across a range of parameter values.

The measured data being used for comparison is that of figures 4.47 and 4.48, this gives the best combination of measured data. The gate S-parameters of figure 4.47 were chosen because they contain the valuable low frequency information essential for obtaining a good fit. Although the data is for two different devices, if the gate data for FET 1#7 in figure 4.47 is compared to that to that in 4.49 for FET 1#14 above 4GHz, where the low value d.c. blocks are having little effect, the results are seen to be reasonably repeatable at each bias level.

The channel and electrode resistances were set using d.c. measurements and 0.1GHz S-parameter data. The depletion resistance was assumed to be constant with reverse bias and set to a typical value [75] of 1.4Ω, 2.1mΩ.m in distributed units, leaving the depletion capacitance as a variable parameter. The model parameters are listed below with their initial values

Depletion Capacitance	Channel Resistance
$C_{dep(zero\ bias)} = 600pF/m$	$R_{ds(zero\ bias)} = 6m\Omega.m$
$C_{dep(mid\ bias)} = 450pF/m$	$R_{ds(mid\ bias)} = 0.24\Omega.m$
$C_{dep(pinch-off)} = 210pF/m$	$R_{ds(pinch-off)} = 90\Omega.m$

Electrode Resistance	Depletion Resistance
$R_g = 103.7K\Omega/m$	$R_{dep} = 2.1m\Omega.m$
$R_s = 844\Omega/m$	
$R_d = 844\Omega/m$	

Connection Inductances

L_c=0.3nH

The results in figures 4.55 to 4.60 show a spread of depletion capacitance values for all S-parameters at three bias levels and compares them to measured data.

Firstly the mid bias state was optimized. The source - drain results are shown in figure 4.55, the gate results in 4.56. The modelled source - drain S-parameters at mid bias show that the reflection coefficient, backward coupling and through transmission are relatively insensitive to variation in the depletion capacitance. However, the forward coupling is seen to be very dependent upon the depletion capacitance. As the capacitance decreases, the resonant frequency increases. The gate S-parameters, show that both the forward and backward coupling on the gate line are relatively insensitive to depletion capacitance. The through transmis-

sion shows resonant behaviour and again the resonant frequency increases with decreasing capacitance. This dual resonant behaviour enables good fitting of the model and highlights well how the combination of all S-parameters helps in the fitting of measured to modelled data. The resonances are observed to have much lower measured Q than modelled, however, it must be remembered that the forward coupling, being at a low level is very susceptible to phasor cancellation and addition effects with signals reflected from the backward coupled port, port 3. Thus any minor differences in the phase relationships between modelled and measured data could produce quite large differences, at these low levels, in magnitude data. The optimum fit was found to be with C_{dep}=250pF/m.

The pinched-off S-parameters were then optimized and are shown in figures 4.57 and 4.58. The source - drain S-parameters show no large dependence upon depletion capacitance. In this state the resistive and capacitive coupling between the source and drain lines is at a minimum and the S-parameters will be more dependent upon electrode geometry. The optimum fit is difficult to determine from these alone, however, the gate S-parameters show strong dependence and allow good fitting. The best fit was found to be 87pF/m. This is much lower than the initial estimate, however, the empirical expression used in section 4.3.4 was a very simple approach. The foundry data which gave C_{dep}=250pF/m was for a 4x75μm FET fabricated using a different implant type [24] and thus could be very different from the devices measured here.

Finally the zero bias state was optimized, shown in figures 4.59 and 4.60 and again little variation is observed for the source drain S-parameters. The small channel resistance of 6mΩ.m is dominating the low frequency region of the S-parameters. The through transmission of the gate S-parameters again allows good optimization to be performed. The best fit was chosen as 500pF/m.

Thus the model has been fitted to the measured data reasonably well at three different bias levels, from 0.1GHz to 20GHz. The optimized model parameter values are summarized below

Depletion Capacitance	Channel Resistance
$C_{dep(zero\ bias)} = 500pF/m$	$R_{ds(zero\ bias)} = 6m\Omega.m$
$C_{dep(mid\ bias)} = 250pF/m$	$R_{ds(mid\ bias)} = 0.24\Omega.m$
$C_{dep(pinch-off)} = 87pF/m$	$R_{ds(pinch-off)} = 90\Omega.m$

Electrode Resistance	Depletion Resistance
$R_g = 103.7K\Omega/m$	$R_{dep} = 2.1m\Omega.m$
$R_s = 733\Omega/m$	
$R_d = 733\Omega/m$	

Connection Inductances

L_c=0.3nH

Conclusions

Improved performance for a wide FET used as a voltage controlled directional coupler has been obtained by reducing the parasitics of the mounting circuit to a minimum. The new test fixture enabled full six-port characterization to be performed, in which the gate associated S-parameters where measured, this led to enhancements in the model whereby electrode resistance was included. The gate S-parameters tended to have strong dependence on bias level and this greatly improved the data fitting procedure. Reasonably good agreement has been obtained for all measured S-parameters at three different bias levels from 0.1GHz to 20GHz.

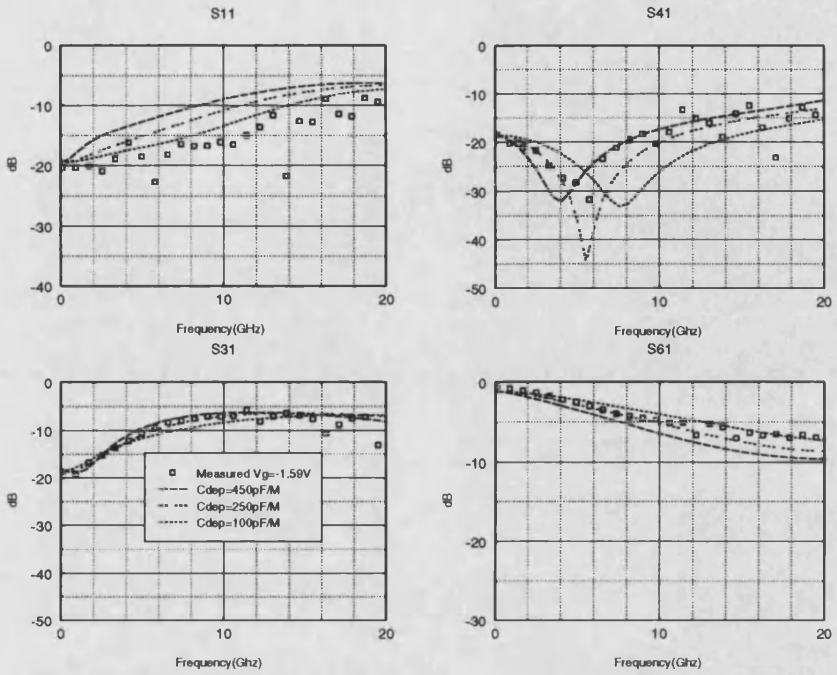

Figure 4.55: Comparison of measured and modelled source - drain S-parameters at mid bias showing variation with depletion capacitance

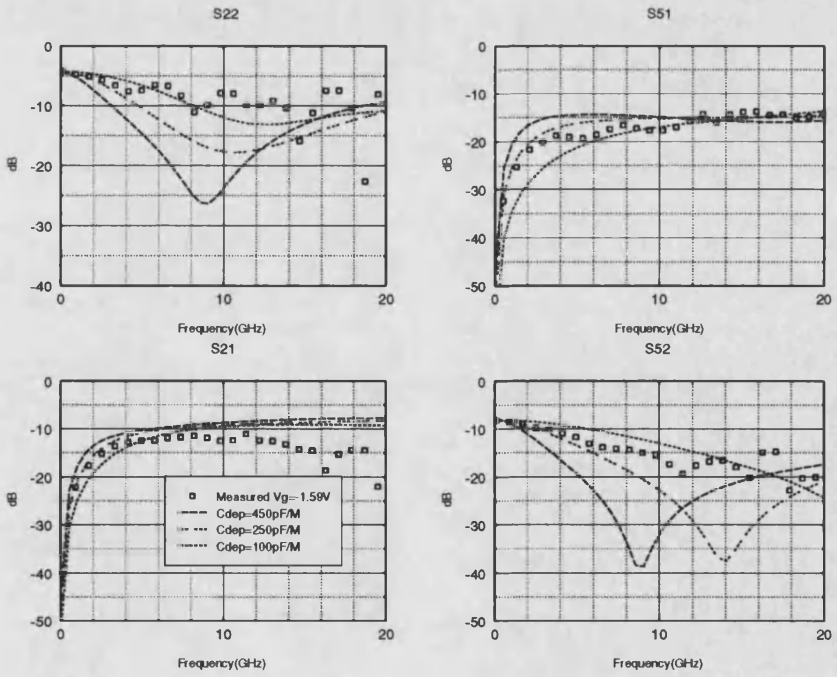

Figure 4.56: Comparison of measured and modelled gate S-parameters at mid bias showing variation with depletion capacitance

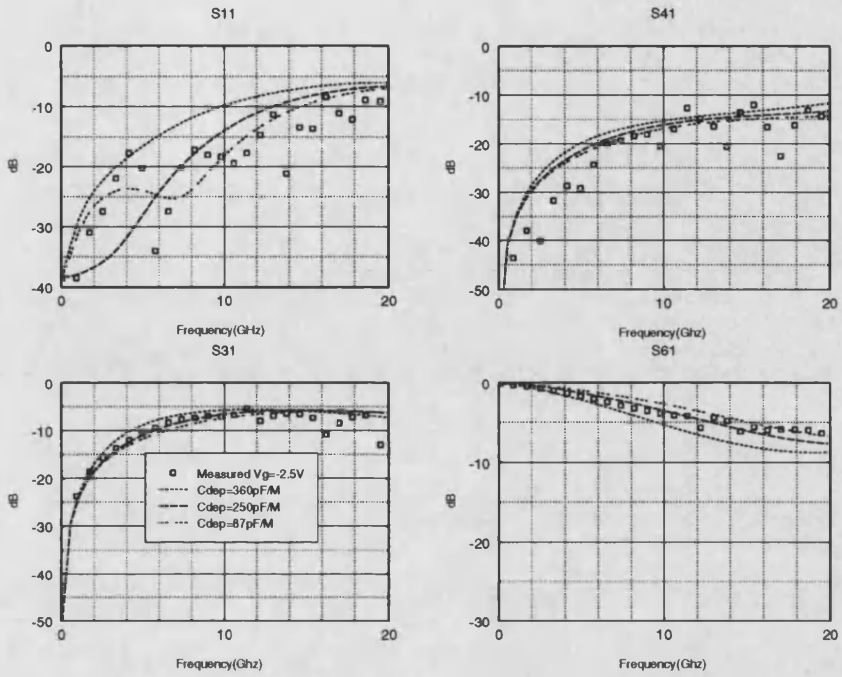

Figure 4.57: Comparison of measured and modelled source - drain S-parameters at pinch-off showing variation with depletion capacitance

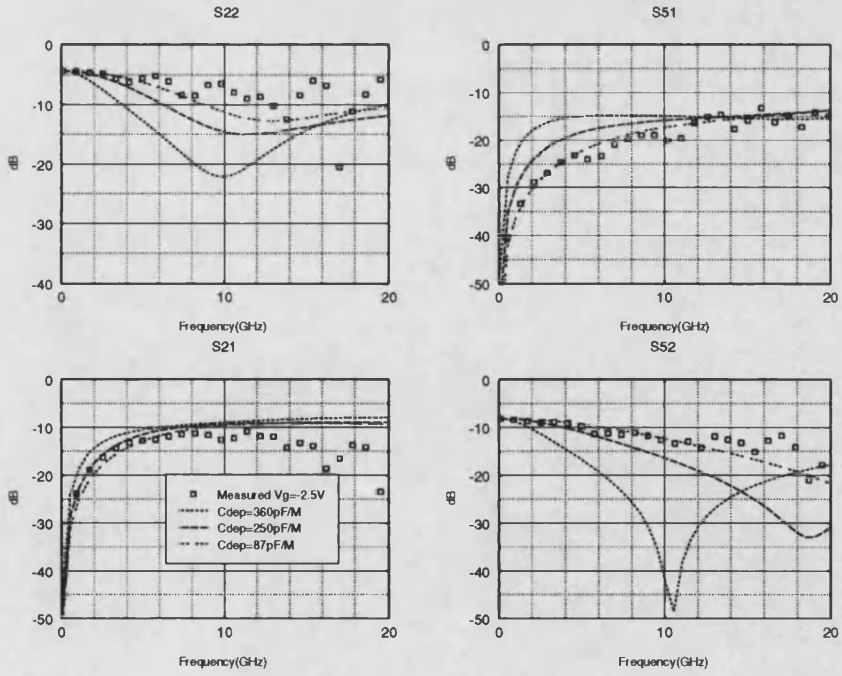

Figure 4.58: Comparison of measured and modelled gate S-parameters at pinch-off showing variation with depletion capacitance

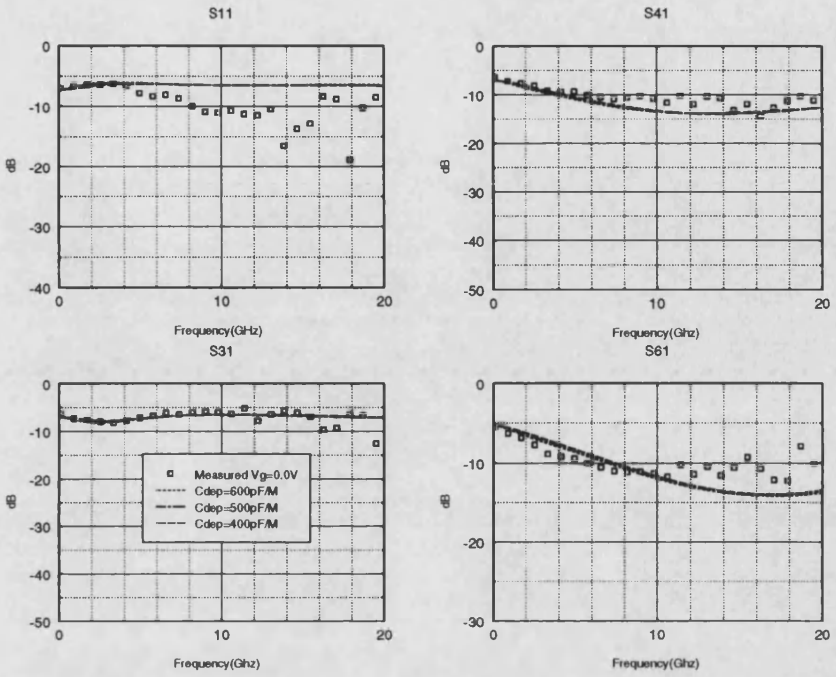

Figure 4.59: Comparison of measured and modelled source - drain S-parameters at zero bias showing variation with depletion capacitance

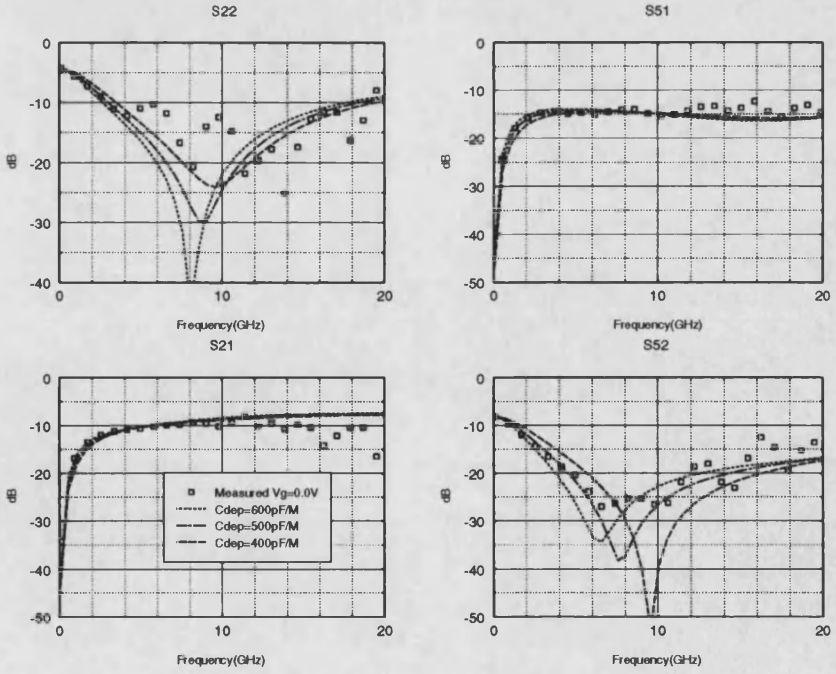

Figure 4.60: Comparison of measured and modelled gate S-parameters at zero bias showing variation with depletion capacitance

4.4 Summary

In this chapter a detailed investigation has been performed on an initial wide FET design. The main feature of the chapter is the improvement in the test fixture performance and the improvements in measurements and modelling that this led to. The basic model of chapter 2 was used to investigate different gate line terminations, this predicted improved performance with 50Ω terminations, this was carried out and found to be the case. The idea of a 50Ω terminated gate line led to full six port characterization, which in turn led to further model enhancements whereby electrode resistances were included. This highlights the interactive nature of the measurement and modelling process, where refinements in one lead to improvements in the other.

In the final test fixture shown in figure 4.42 directional coupler performance is obtained which is comparable with commercially available microstrip couplers [101]. Not only is the directivity of the coupler reasonable, 10dB from 4.0GHz to 10.75GHz but over part of this band it is tunable with gate bias. This allows for optimum directivity to be tuned to a specific band giving enhanced coupler performance. This tunable directivity would also allow for post-fabrication tuning of devices to meet rigorous directivity specifications, which would improve device yield.

The basic model developed in chapter 2 has been enhanced and has been fitted to measured data, resulting in resonably good agreement. The model can now be used to predict the performance of other electrode geometries in the way the basic model was used in this chapter. In the next chapter the performance of this improved model will be tested with comparisons to other wide FETs with different electrode geometries.

Chapter 5

FET Structure Iterations and Model Improvements

5.1 Introduction

The nature of MMIC design is a long turnaround time, from design to chip fabrication can take up to five months. For multi-project wafer designs, such as used in this work, the timing of design runs is controlled by the foundry, for GMMT this is every three to four months. This implies that if a design run is missed, this can delay obtaining a fabricated device by up to eight months. For this reason the first iteration design (FET 2) was undertaken prior to the electrode geometry optimization discussed in the previous chapter, the optimized device (FET 3) will be the subject of the next section.

The first two sections present measured and modelled results for FETs 2 and 3. The final section then introduces improvements to the model which result in good agreement between measured and modelled data for all three FET structures.

5.2 The Second Wide FET Structure

5.2.1 Introduction

The device to be discussed in this section is denoted FET 2 and was the first design carried out as part of this work, funded by a Eurochip quota award. The foundry process had been updated since the first design and is known as the F20 process [24], this uses gate lengths of 0.5μm, allows the use of via holes and gives usable FET performance up to 20GHz.

The design was again based around standard foundry components, and as in the FET 1 design the basic building block was the 300μm single gate fingered FET. In the F20 process the source and drain lengths had been reduced from 38μm to 22μm, it was decided to use these new electrode dimensions. The main reason for this was that the process used to fabricate the first FET was very different from the F20 process used for the second and a comparison of devices with identical source and drain geometries would not produce identical electrical results. Thus, while ideally only one parameter would be varied between iterations, in this case it was not possible. Having decided on source and drain lengths, the other variable parameter of device width had to be chosen. While keeping the device length constant was an option, it was felt that because of the length of design turnaround, it would be beneficial to have as many measured parameter variations as possible in order to test the validity of the model. It was thus decided to increase the device length to 2.0mm, intuitively this would reduce the frequency of distributed coupling effects and would reduce the effect of circuit parasitics on device performance.

The FET electrode structure is summarized below

Source length = 22μm

Drain length = 22μm

Gate length = 0.5μm

Drain to Gate spacing = 2.3μm

Source to Gate spacing = 2.3μm

Device width = 2000μm

To obtain a device width of 2.0mm, six standard 300μm devices were connected in parallel, the layout of the device is shown in figure 5.1

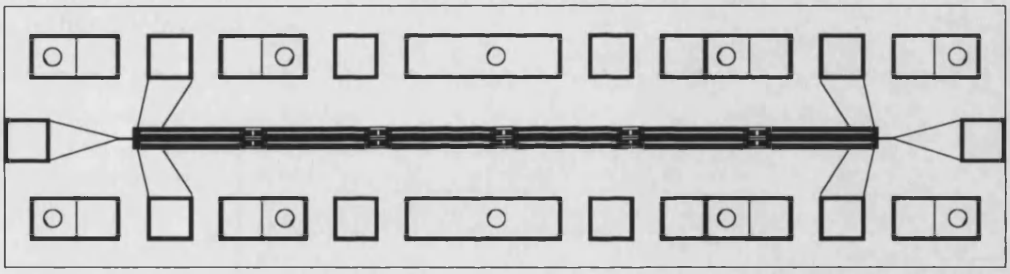

Figure 5.1: Second wide FET test structure

The configuration is the same as for the first design, with 120μm bond pads at either end of source, gate and drain lines. However, since in the F20 process through vias were available, it was decided to allow for on-wafer probing. This involved placing grounded bond pads on either side of the signal bond pad to facilitate coplanar tip probing which is the common standard [24]. The via holes are marked as circles on the layout. It is also seen that the feed lines from the source and drain bond pads have been widened to reduce any inductive effects.

In this section a d.c. characterization of two wide FETs is carried out and the results compared to those of FET 1. Microwave characterization is then performed on two devices. Six-port S-parameters are measured, firstly using low value d.c. blocking capacitors and a transmission line choke. The transmission line choke is then replaced by a choke coil and finally, high value d.c. blocking capacitors and choke coils are used. The model developed in the preceding chapter is then used to fit the measured data, and conclusions drawn.

5.2.2 D.C. Characterization

As for the FET 1 devices, two FET 2 devices were mounted in microwave test fixtures to allow both d.c. and microwave characterization. The output and transfer d.c. results are shown in figures 5.2 and 5.3

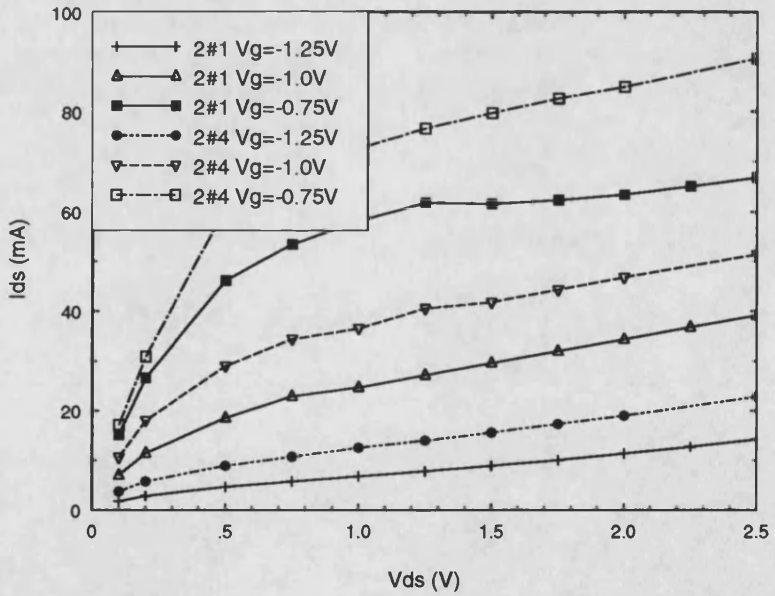

Figure 5.2: Output I-V characteristics for FET 2#1 and FET 2#4

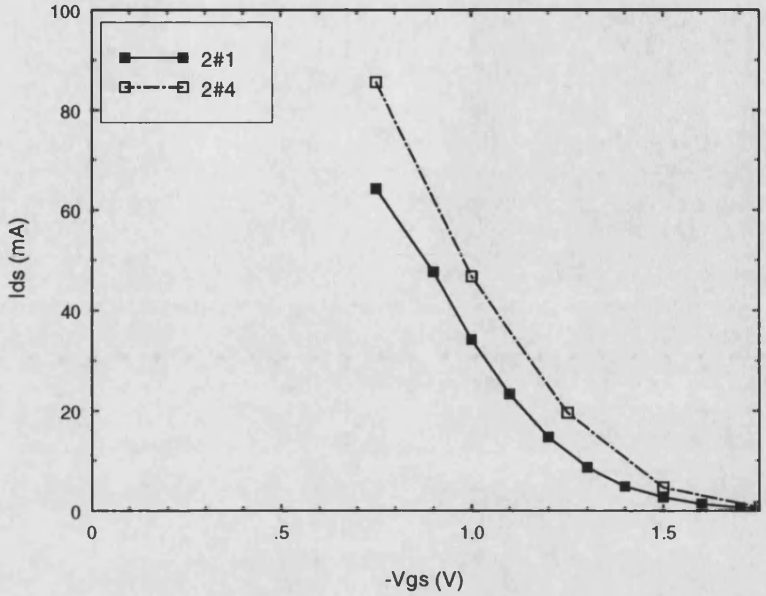

Figure 5.3: Transfer I-V characteristics for FET 2#1 and FET 2#4

Typical FET characteristics are observed in both cases. A large spread in results is observed, as with the FET 1 devices shown in figures 4.12 and 4.13. The d.c. parameters were calculated and are shown below in table 5.1

	GMMT 1 X 300μm			FET 1		FET 2	
	min.	typ.	max.	FET 1#3	FET 1#7	FET 2#1	FET 2#4
I_{dss} (mA)	30	45	60	134	117	148	196
g_m (mS)	20	30	40	100.8	95.5	113	129
R_{ds} (Ω)		640		100	150	272	98
V_p (V)	-1.2	-1.8	-2.5	-1.57	-1.45	-1.75	-1.8

Table 5.1: D.C. parameters of FET 1 and FET 2 compared with GMMT data

For the FET 2 devices, the transfer results were measured at V_{ds}=2.0V, this was felt to be a reasonable operating point for the device, g_m was calculated at V_{gs}=-1.0V. R_{ds} was measured at V_{ds}=1.8V and V_{gs}=-0.75V. There is reasonable agreement with the expected trends, in that g_m and I_{dss} should be proportional to gate length. The pinch-off voltage is within the range specified by the manufacturer. The output resistance for FET 2 is seen to be lower than for the single 300μm device. For six devices in parallel the resistance would be of the order of a sixth of the single device value, as in the case of FET 2#4. The higher

value for FET 2#1 may be due to the very wide gate of FET 2. In general, however, the d.c. parameters of the FET 2 devices show good agreement with expected trends and as with FET 1, show that these devices are typical of those produced by the foundry.

5.2.3 Microwave Characterization of FET 2

Introduction

In this section the full six-port S-parameters of two FET 2 devices will be presented and compared with those of FET 1. All the improvements to the test fixture implemented through section 4.3.6 are shown, starting from high impedance transmission line chokes and low value d.c. blocking capacitors and concluding with coil choking and high value capacitors. Finally a second device is measured as a repeatability check.

Measured Results

The first of these devices, FET 2#1 was mounted in the updated test fixture shown in figure 4.42. The source - drain S-parameters are shown below

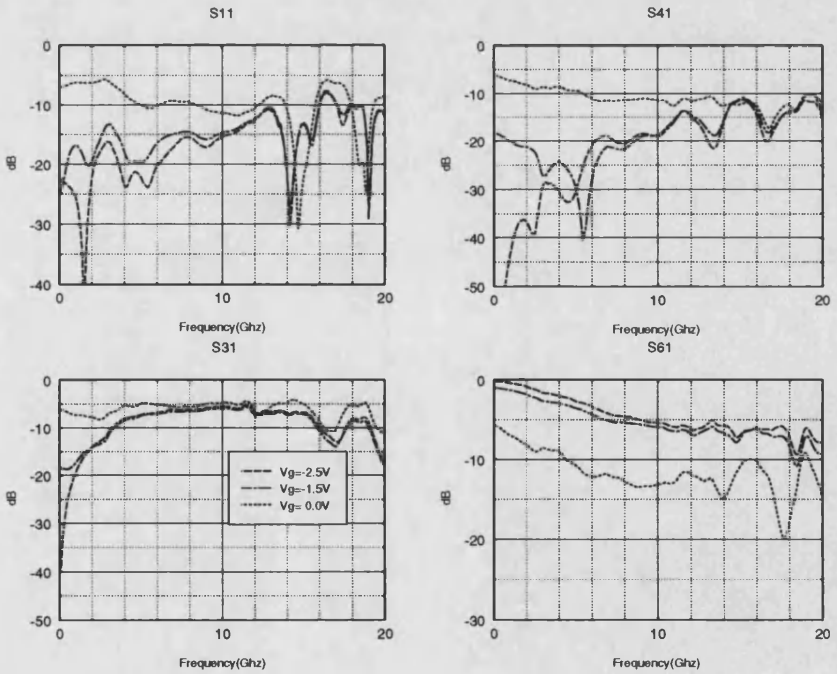

Figure 5.4: Source - drain S-parameters for FET 2#1 with transmission line choke and 5.6pF d.c. blocks

As with FET 1 backward coupling is observed, and the forward coupling exhibits a resonant behaviour at the mid bias point. Comparing these results to those for FET 1 in the same test fixture, shown in figure 4.43, there are a number of points to note. Firstly, the resonance in S_{41} is much sharper and is at slightly lower frequency as was intuitively predicted. The backward coupling is seen to be slightly higher for FET 2, at 10GHz FET 1 gives -7dB, whereas FET 2 gives -6dB. This agrees with the trend predicted by the basic model in section 4.3.5 and shown in figure 4.34. As in that case this increase in backward coupling leads to a decrease in through transmission for FET 2. The reduced length of the source and drain lines from 38μm to 22μm will result in higher d.c. resistance, also giving decreased through transmission. The reflection coefficient of FET 2 is generally of the same order as for FET 1$\simeq$ -15dB to -20dB below 10GHz.

The gate associated S-parameters were also measured and are shown below

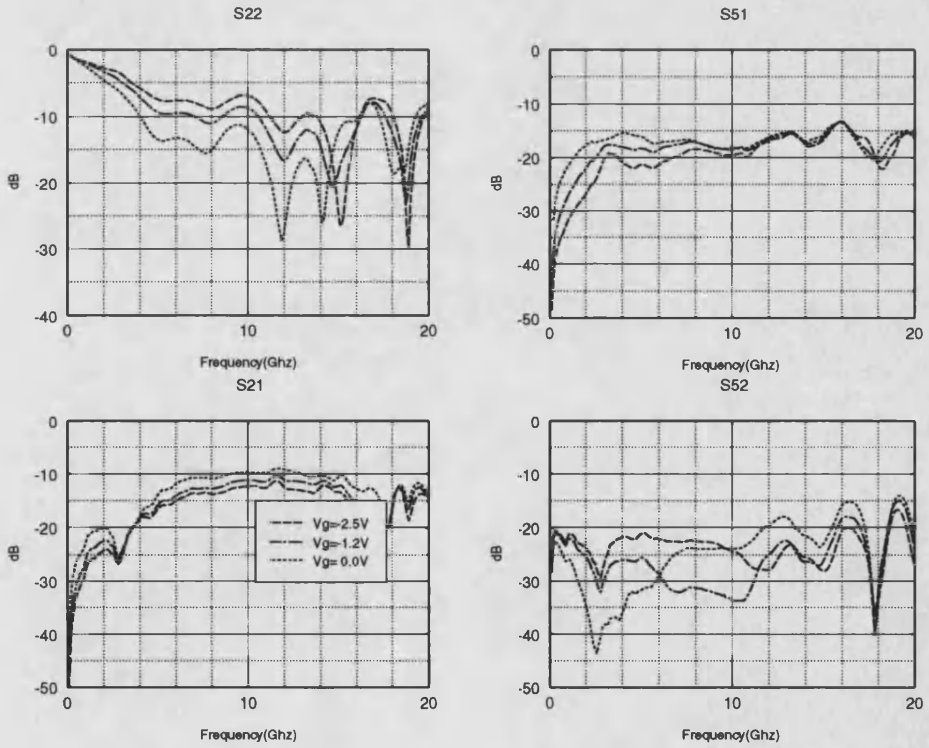

Figure 5.5: Gate S-parameters for FET 2#1 with transmission line choke and 5.6pF d.c. blocks

Initially the mid bias point was set differently for the gate S-parameter in order to show

the range of variation. In later measurements all S-parameters were taken at the same bias point. The general form of the S-parameters is the same as that for FET 1 shown in figure 4.46. The main difference is the much lower level of the through transmission, caused by the smaller cross section of the gate line. The trend for FET 2 is also different in that the pinched-off through transmission is not the highest of the three bias levels. Again, however, the S-parameters are being dominated by the effect of the bias circuits.

The transmission line choke was replaced with a wire wound choke and the S-parameters remeasured. The source - drain results are shown below.

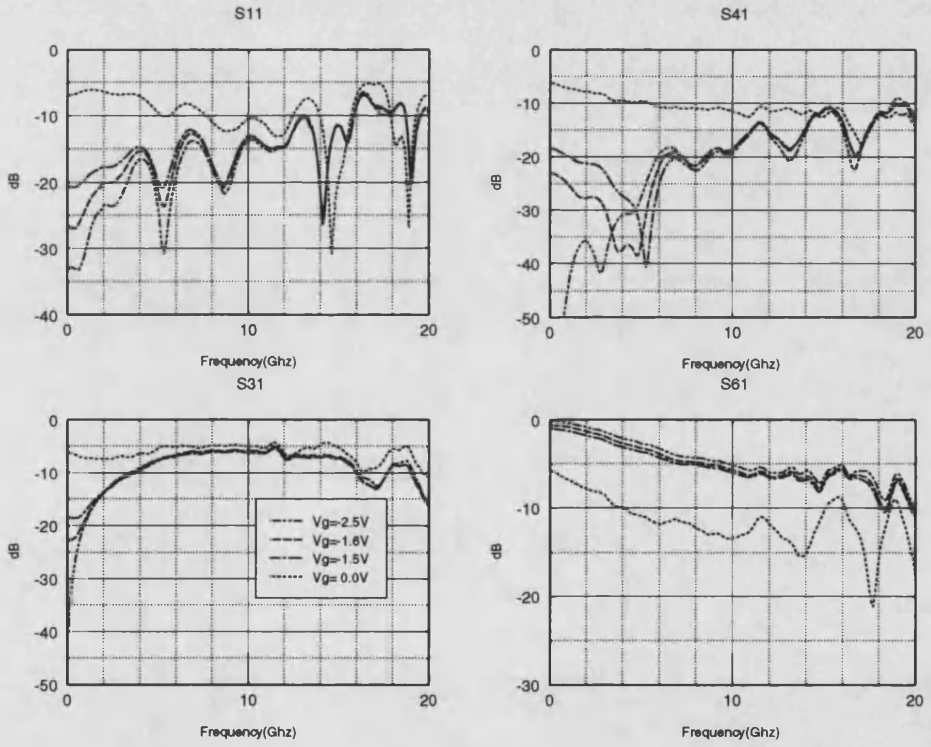

Figure 5.6: Source - drain S-parameters for FET 2#1 with coil choke and 5.6pF d.c. blocks

As with FET 1 there are few differences in these results with the addition of the choke coil. The sharp resonance at V_g=-1.5V is well reproduced. An extra bias level of V_g=-1.6V has been added to show the extent to which the resonance can be tuned. It is seen that 2GHz to 3GHz tuning bandwidth is obtained, the directivity results will be plotted subsequently for comparison with FET 1 results. The reflection coefficient has been degraded slightly, this

may have been caused by slight damage to tape bond connections during the addition of the choke coil. The level is still reasonable, at ≃-13dB to 10GHz.

The gate S-parameters show the benefit of choke coil biasing, shown here in figure 5.7

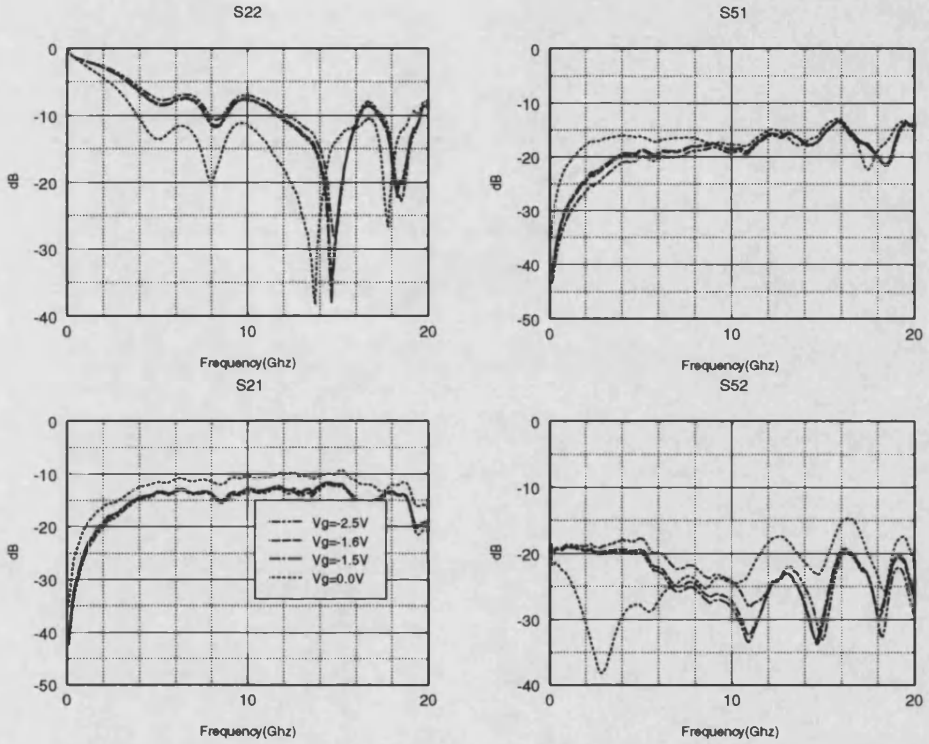

Figure 5.7: Gate S-parameters for FET 2#1 with coil choke and 5.6pF d.c. blocks

The sharp bias circuit resonances have been removed, revealing smooth forward and backward coupled responses. Backward coupling is again observed. The through transmission retains a resonance around 3GHz, similar behaviour is observed in FET 1 shown in figure 4.47, the resonance there being at higher frequency, ≃ 8GHz.

In order to obtain measured data with a low frequency response that is unaffected by the gate bias circuits, high value d.c. blocking capacitors are required, 56pF single layer ceramic capacitors were obtained and replaced the 5.6pF capacitors. The results are shown below

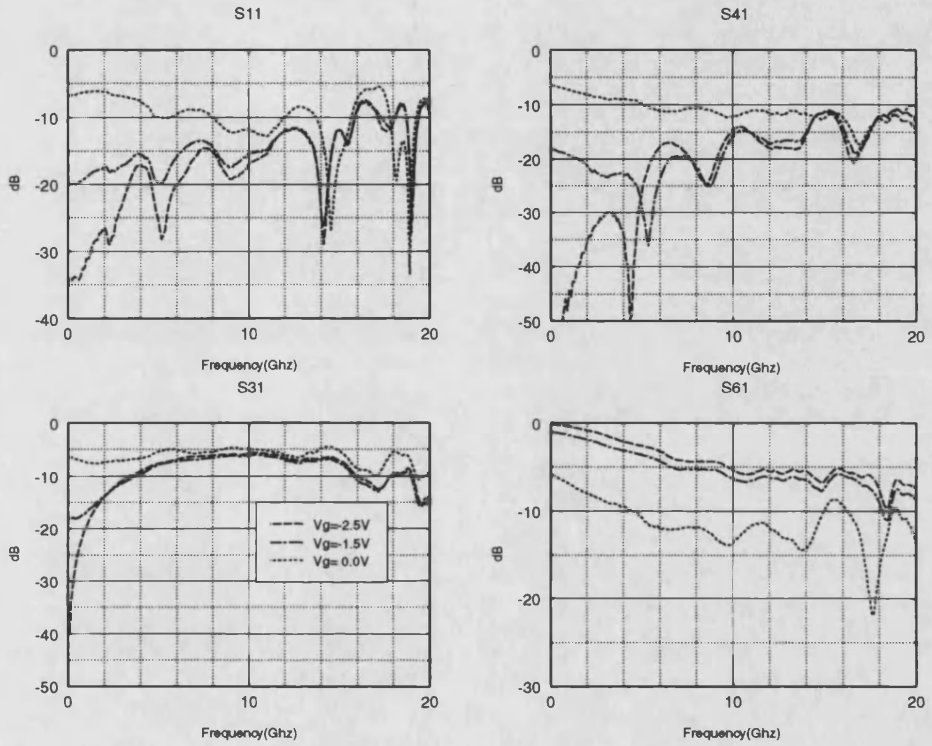

Figure 5.8: Source - drain S-parameters for FET 2#1 with coil choke and 56pF d.c. blocks

Comparing these with figure 5.6, it seen that all the results are very similar. However, the forward coupling is slightly worse in this case. The mid bias resonance is at the same frequency, but at a higher level. This shows the sensitivity of the source - drain forward coupling to the changes in the gate terminations. The forward coupling, in both the pinched-off and mid bias states exhibits a large rippling effect. As discussed in chapter 3, this often occurs in microwave circuits and is caused by the phasor addition of two signals with different path lengths. The ripple frequency is easily related to the difference in path length, an expression for this is given in chapter 3. The ripple frequency observed here suggests a two-way path difference of $\simeq$14mm on the microstrip mounting circuit, this is approximately the length of the microstrip input lines. Thus it would seem that power is coupling to port 3, reflecting from the SMA/microstrip transition and passing to port 4, where is it rippling with

the direct forward coupled signal. The actual forward coupled signal will be less than that shown in figure 5.8, up to a maximum of 6dB less if the two signals are of the same amplitude. Taking this effect into account, the improvement in the mid bias directivity is greater for the 56pF d.c. blocks in the 6GHz to 8GHz region than for the 5.6pF d.c. blocks. The directivity in the pinched-off state is also greater with 56pF d.c. blocks. This highlights the problems associated with the measurement of multiport devices with non-ideal connections.

The more interesting results were for the gate line shown in figure 5.9

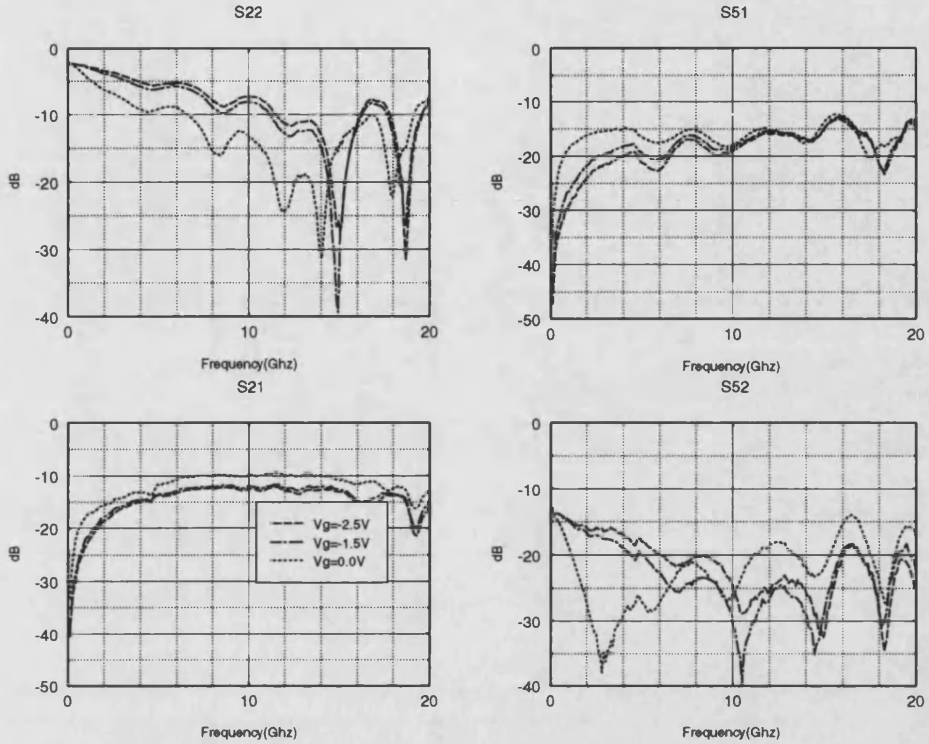

Figure 5.9: Gate S-parameters for FET 2#1 with coil choke and 56pF d.c. blocks

These results show the low frequency S-parameters unaffected by the bias circuits. The through transmission is seen to be very different, $\simeq$ 5dB greater at 0.1GHz. Comparing the through transmission results to those for FET 1 using the HP8510 internal bias tees, shown in figure 4.47, the same monotonic increase at low frequency is observed, showing that the 56pF capacitors are having very little effect.

As a repeatability check, another device was mounted in this configuration and the full S-parameters measured. The source - drain S-parameters are shown below

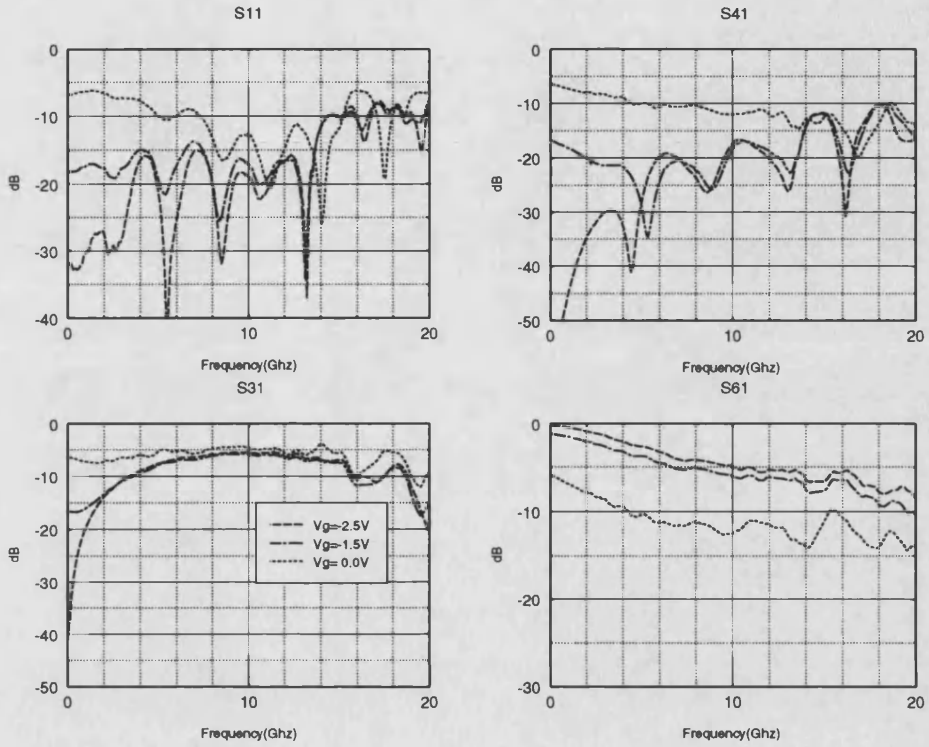

Figure 5.10: Source - drain S-parameters for FET 2#4 with coil choke and 56pF d.c. blocks

Comparing these with figure 5.8, the resonance in the forward coupling is at the same frequency and very similar amplitude. The forward coupling at pinch-off is $\simeq$3dB lower around 6GHz for FET 2#4 than for FET 2#1, this could be due to the repeatability of the test fixture assembly as well as the device itself. This highlights the advantage of on-chip probing where very repeatable connections can be obtained. It is observed that at Vg=-1.5V the two devices have different S-parameters at 0.1GHz, showing the spread in the d.c. parameters of these devices already observed in the d.c. characterization section.

The gate results are shown below

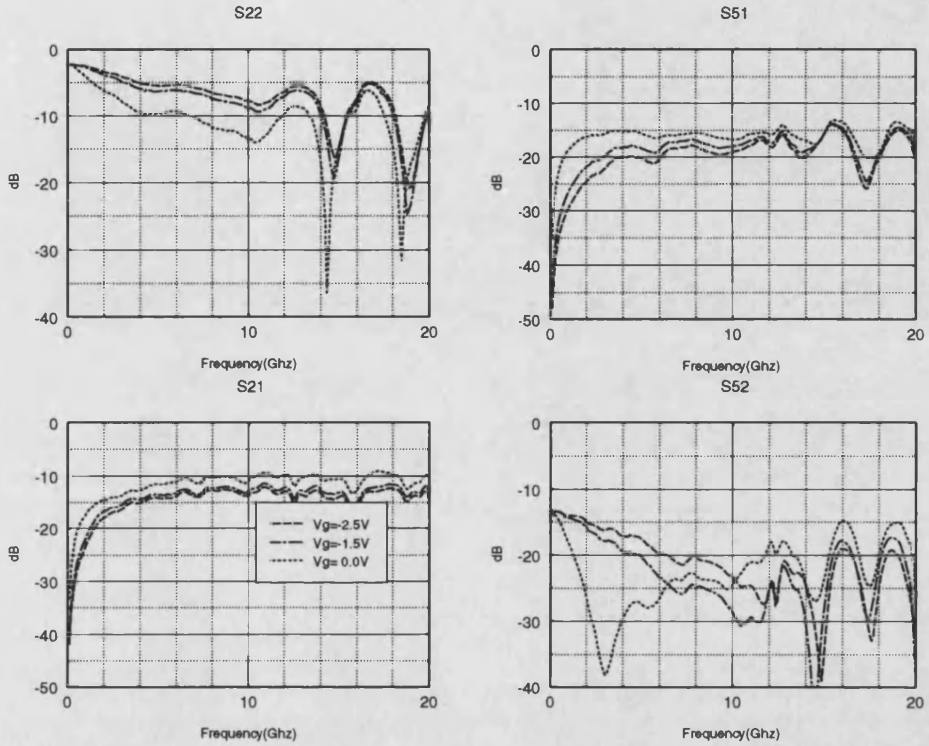

Figure 5.11: Gate S-parameters for FET 2#4 with coil choke and 56pF d.c. blocks

Comparing the results to those of figure 5.9 again good repeatability is observed, the through transmission resonance at zero bias is at the same frequency.

As with FET 1 the directivity of the source - drain was calculated for comparison. The results for FET 2#1 with 5.6pF d.c. blocks were used since they show the high performance obtainable from these devices. The directivity is shown below along with backward coupling.

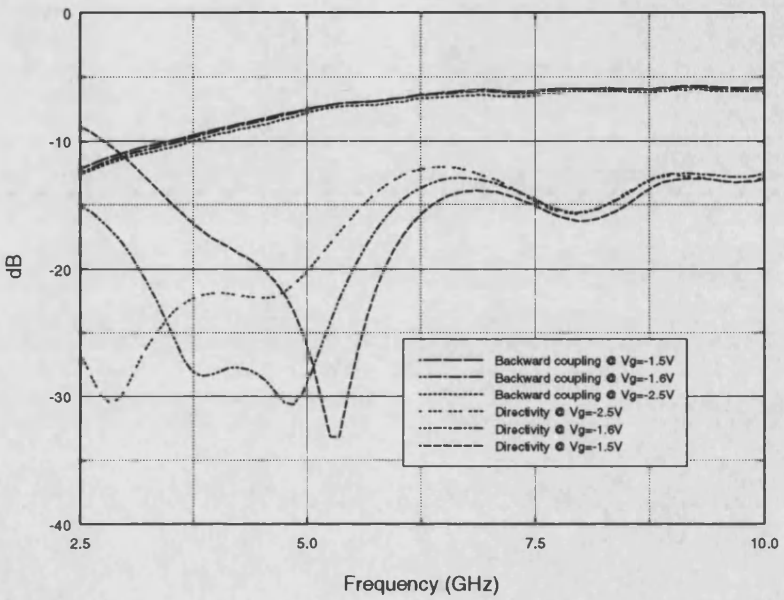

Figure 5.12: Directivity and backward coupling for FET 2#1 with transmission line choke and 5.6pF d.c. blocks

The band of optimum performance, in terms of coupling flatness and directivity was chosen as 2.5GHz to 10GHz. The coupling flatness across this band is ± 3.5dB and the directivity is >12dB (plotted as a negative quantity for convenience). Comparing this to FET 1 results shown in figure 4.44, it is seen that while the coupling flatness is worst than the ±2.2dB for FET 1, the directivity has improved from 10dB to 12dB. However, the major feature of the FET 2 results is the tunability obtained in the lower frequency range. Directivities >25dB can be obtained from 2.5GHz to 5.6GHz with the aid of tuning at a coupling flatness of ±2.65dB. This performance compares well with that quoted for commercial microstrip directional couplers, MA-COM specify a 10dB coupler from 2.6GHz to 5.2GHz with ±1.0dB flatness and 20dB minimum directivity [101].

The through transmission and reflection coefficient are shown below for this band

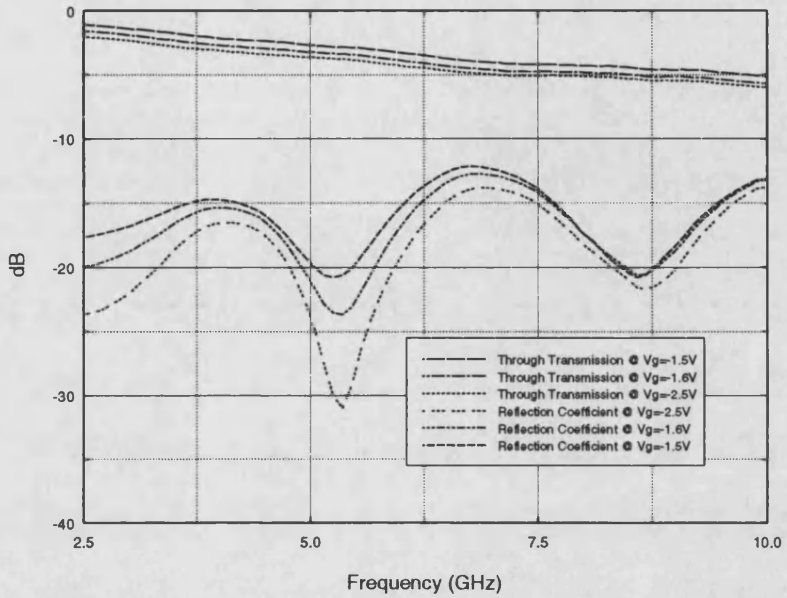

Figure 5.13: Through transmission and reflection coefficient for FET 2#1 with transmission line choke and 5.6pF d.c. blocks

The through transmission is again low as with the results for FET 1 shown in figure 4.45, it is hoped with the aid of the model developed in this work to improve upon this performance. The reflection coefficient is reasonable being <-12dB.

Conclusions

Two FET 2 devices have been fully characterized and show improved performance in terms of tunable directivity when compared to the FET 1 device. The through transmission and coupling flatness performance is less good for FET 2, it is hoped that using the model being developed in this work this performance can be improved. The measured data shown in this section was then used for fitting of the model, these results are presented and discussed in the next section

5.2.4 Modelling of FET 2

Introduction

The model developed in chapter 2 and improved in section 4.3 will be fitted to the data for the FET 2 device shown in the preceding section. Initially the inter-electrode capacitances of the structure are calculated. Then using low frequency S-parameter measurements and d.c. resistance measurements the electrode series resistances and channel resistances are obtained. The depletion capacitance is then varied to obtain best fit to the measured data.

Modelling Results

The geometry of the FET electrodes is given below

Source length = 22μm
Drain length = 22μm
Gate length = 0.5μm
Drain to Gate spacing = 2.3μm
Source to Gate spacing = 2.3μm
Device width = 2000μm

The inter-electrode capacitances for the structure were calculated using the resistance network analogue. The reduced length of the source and drain electrodes allowed three nodes to be placed across the 0.5μm gate line, whilst maintaining a reasonable sized reduced matrix for inversion.

The resistance of the gate line was measured and found to be 325Ω, this is equivalent to 162.5KΩ/m. The resistance of the source and drain electrodes was found to be 800Ω/m, which is higher than the FET 1 value of 733Ω/m as expected. The zero bias channel resistance was measured as 4.0Ω, as for FET 1, this gave a distributed value of 8mΩ.m, the mid bias

and pinched-off channel resistances were given the same total values as for FET 1, since the S-parameters at 0.1GHz were to be set at the same values as for FET 1, in distributed units these were, 0.32Ω and 120Ω.m respectively. The depletion capacitances were set at reasonable levels and the depletion resistance and connection inductances remained the same as for FET 1. The parameter values are summarized below

Depletion Capacitance	Channel Resistance
$C_{dep(zero\ bias)}$ = 500pF/m	$R_{ds(zero\ bias)}$ = 8mΩ.m
$C_{dep(mid\ bias)}$ = 300pF/m	$R_{ds(mid\ bias)}$ =0.32mΩ.m
$C_{dep(pinch-off)}$ =200pF/m	$R_{ds(pinch-off)}$ = 120Ω.m

Electrode Resistance	Depletion Resistance
R_g = 162.5KΩ/m	R_{dep} = 2.1mΩ.m
R_s = 800Ω/m	
R_d = 800Ω/m	

Connection Inductances

L_c=0.3nH

The measured data used for comparison was that of figures 5.8 and 5.9, it was felt that these results showed the typical performance of the FET 2 devices rather than the 5.6pF d.c. block results which show slightly improved performance. The S-parameters were simulated at different C_{dep} values and the results are shown in figures 5.14 to 5.19.

The mid bias state S-parameters are shown in figures 5.14 and 5.15. The source - drain S-parameters show similar trends to the FET 1 device, in that only the forward coupling shows a large sensitivity to C_{dep}. The resonant frequency again increases with increasing capacitance. The resonance is slightly lower in frequency in FET 2 than FET 1 for the measured data, and more so for the modelled data, as was intuitively predicted because of the increased width of the FET 2 device.

The optimum C_{dep} value is difficult to determine from this data alone, however, the gate S-parameter data shown in figure 5.15 enables the best overall fit to be chosen. The resonant behaviour of the through transmission indicates a best fit with C_{dep}=180pF/m.

The pinched-off source - drain S-parameters are shown in figure 5.16, as with FET 1, there is little variation with C_{dep}. The fit of the model is reasonable, except for the low frequency forward coupling, in the 4GHz region where a 10dB difference is observed. This however, was the best fit obtainable, further improvements to the model to be outlined in later sections will improve this fit. The gate S-parameters shown in figure 5.17 again enabled the best fit to be chosen as C_{dep}=100pF/m.

Finally the zero bias state was optimized, very little variation is observed as the source - drain S-parameters are dominated by the low channel resistance. Using the resonant through transmission of the gate S-parameters, the best fit was chosen as C_{dep}=600pF/m. The optimized model parameters are shown below

Depletion Capacitance	Channel Resistance
$C_{dep(zero\ bias)}$ = 600pF/m	$R_{ds(zero\ bias)}$ = 8mΩ.m
$C_{dep(mid\ bias)}$ = 180pF/m	$R_{ds(mid\ bias)}$ =0.32mΩ.m
$C_{dep(pinch-off)}$ =100pF/m	$R_{ds(pinch-off)}$ = 120Ω.m

Electrode Resistance	Depletion Resistance
R_g = 162.5KΩ/m	R_{dep} = 2.1mΩ.m
R_s = 800Ω/m	
R_d = 800Ω/m	

Connection Inductances

L_c=0.3nH

Conclusions

In this section modelled data has been fitted to measured data for the FET 2 device and a reasonable level of fit has been obtained. The pinched-off forward coupling is not being modelled well at low frequencies, later in this chapter further enhancements to the model are introduced which will improve this fit.

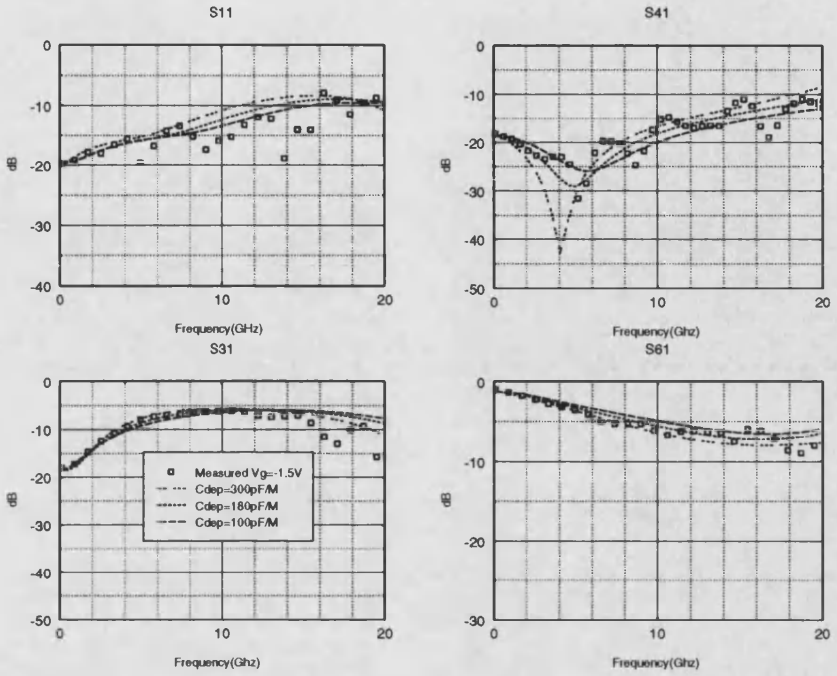

Figure 5.14: Comparison of measured and modelled source - drain S-parameters at mid bias showing variation with depletion capacitance

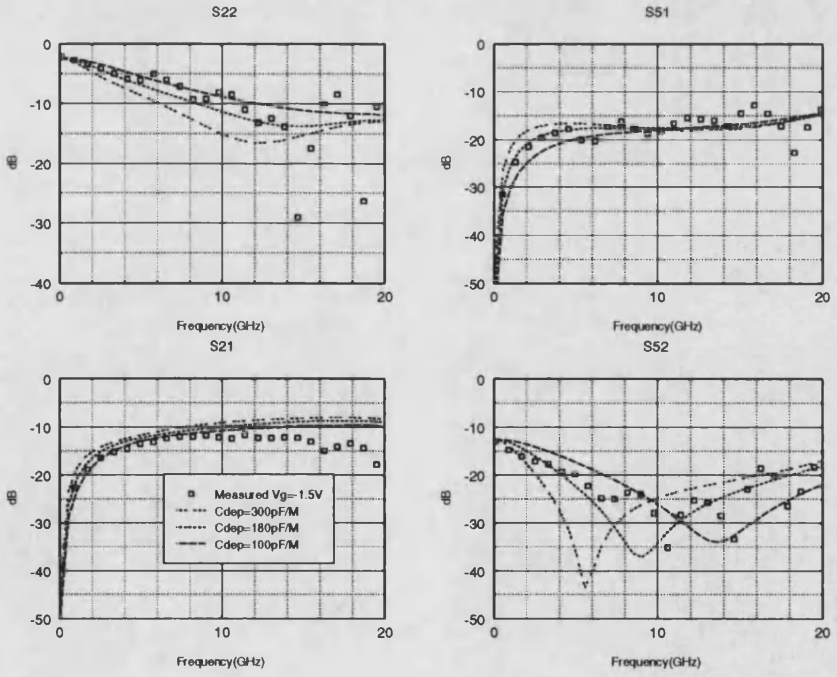

Figure 5.15: Comparison of measured and modelled gate S-parameters at mid bias showing variation with depletion capacitance

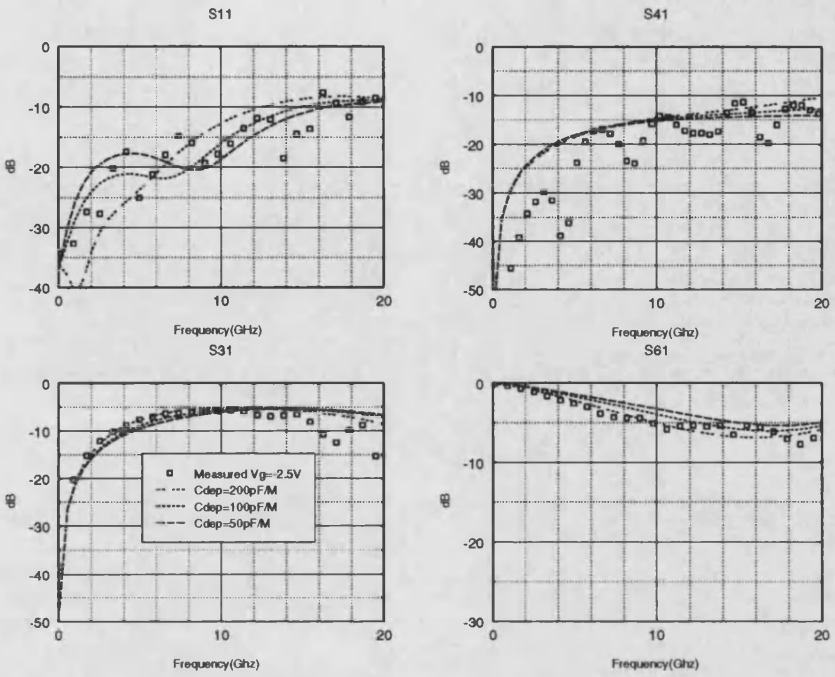

Figure 5.16: Comparison of measured and modelled source - drain S-parameters at pinch-off showing variation with depletion capacitance

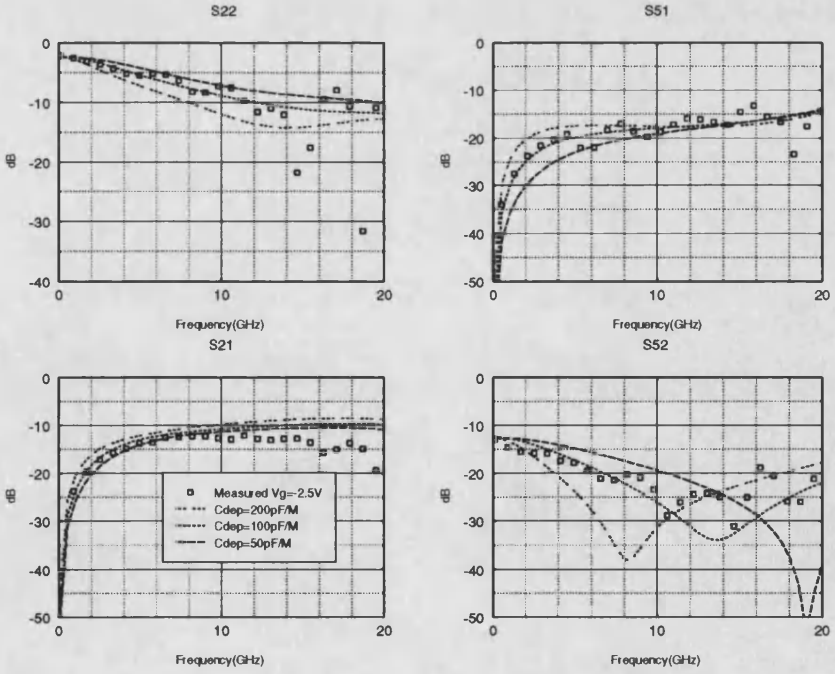

Figure 5.17: Comparison of measured and modelled gate S-parameters at pinch-off showing variation with depletion capacitance

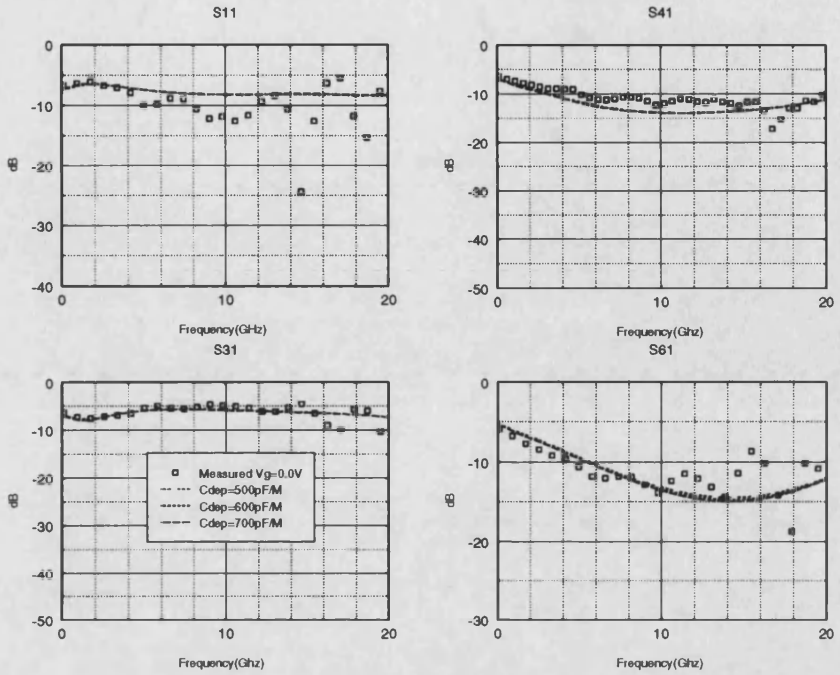

Figure 5.18: Comparison of measured and modelled source - drain S-parameters at zero bias showing variation with depletion capacitance

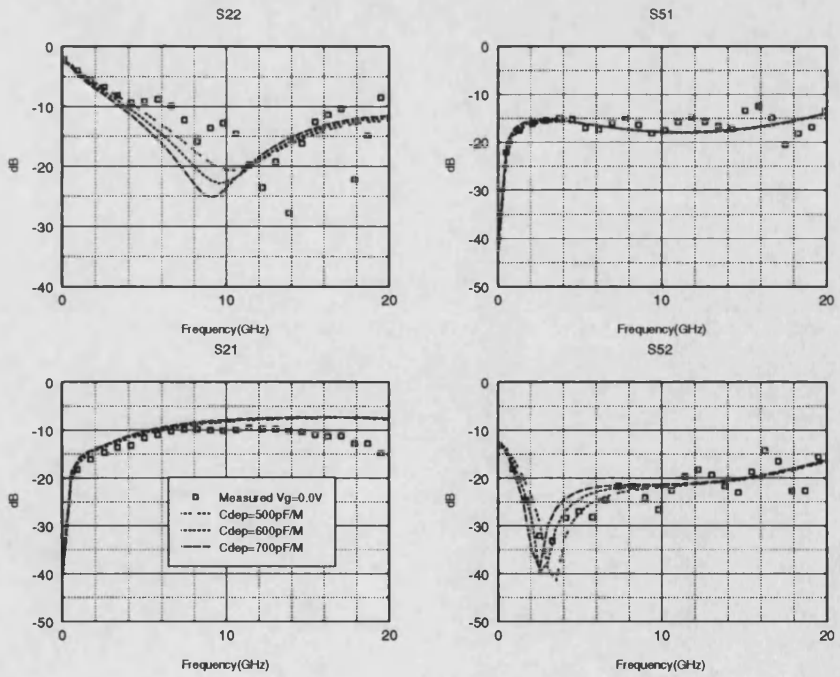

Figure 5.19: Comparison of measured and modelled gate S-parameters at zero bias showing variation with depletion capacitance

5.2.5 Conclusions

A second wide FET structure has been characterized and modelled data has been fitted reasonably well to the measured data. The performance of the device in terms of tunable directivity has been shown to be better than that for FET 1, particularly if only the intrinsic isolation signal is considered and reflections from connector transitions are ignored. For the case of 5.6pF d.c. blocking gate capacitors particularly good performance has been obtained, highlighting the devices sensitivity to gate terminations.

As a repeatability check, two devices have been characterized and show very similar performance. Different S-parameters at 0.1GHz are obtained for the two devices, however, this does greatly affect the microwave repeatability of the devices, in that resonances occur at the same frequency and have very similar amplitudes. The microwave repeatability has been shown to be good, this not only shows that the devices themselves are repeatable but also shows that the microstrip mounting circuit and tape bonding method are also reasonably repeatable.

The FET 2 devices have been made compatible with on-wafer probing, it is hoped in future work to carry out these measurements, and obtain measurements of the intrinsic device performance unaffected by reflections from connector transitions. It is also hoped to include the microstrip mounting circuit, transitions and bias circuits in the modelling procedure to give a more complete insight into the measurements taken in this section.

5.3 The Third Wide FET Structure

5.3.1 Introduction

In this section a wide FET with the optimum electrode structure predicted by the basic model in section 4.3.5 is fully characterized. This device is denoted FET 3 and was fabricated using the GMMT F20 process, funded by a Eurochip quota award.

The source and drain length predicted by the basic model was 90μm, this resulted in a fabricated width of 94μm including the M1 layer metal width. The remaining dimension to be decided was the device width. Having increased the device width in the FET 2 design, it was decided to reduce the width for the FET 3 design to 1.36mm. Intuitively it was felt this would result in higher frequency distributed coupling effects and higher through transmission, the low through transmission measured in FET 1 being a major drawback in its performance. The final electrode geometry is summarized below

Source length = 94μm

Drain length = 94μm

Gate length = 0.5μm

Drain to Gate spacing = 2.3μm

Source to Gate spacing = 2.3μm

Device width = 1360μm

The FET 3 layout is shown below

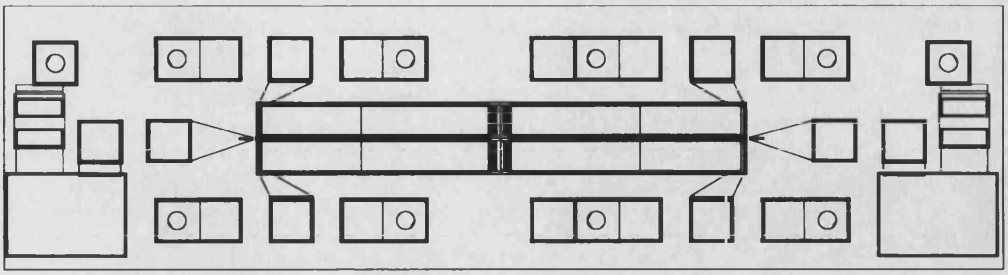

Figure 5.20: Third wide FET test structure

The same basic layout is used again, however, this design no longer uses standard foundry devices. The main difference in the FET 3 design is the reduced number of M2-M3 vias, after discussions with Eurochip and the GMMT foundry it was felt that the yields obtained for FETs 1 and 2 suggested that wider devices could be used. Thus only one via is used to join two devices of $\simeq 600\mu$m width. The source and drain lines are again terminated in 120μm bond pads with ground pads for on-wafer probing. The other feature of note here is the inclusion of on-chip 50Ω resistors. Using the basic model, enhanced performance was predicted with 50Ω gate resistors for all structures simulated in the optimization procedure, thus these were included in the FET 3 design. On-chip d.c. blocks of 36pF were included in series with the gate resistors, the performance of these was found to be good and is shown in chapter 3. The transmission line connections between the source and drain electrodes and the 120μm bond pads form a sharp discontinuities, these were required to keep the area of GaAs used to a minimum. The physical size of these discontinuities was felt to be small enough such that the parasitics associated with them would be very small.

In this section the d.c. characteristics of two devices are presented. These two devices are the measured between 0.1GHz to 20GHz using both on-chip d.c. blocks and gate resistors and external terminations and d.c. blocks mounted on the microstrip circuit. The measured data is then used in fitting of the modelled data. Finally some conclusions are drawn.

5.3.2 D.C. Characterization

Two FET 3 devices were mounted in microwave test fixtures and the d.c. I-V characteristics were measured and are shown below

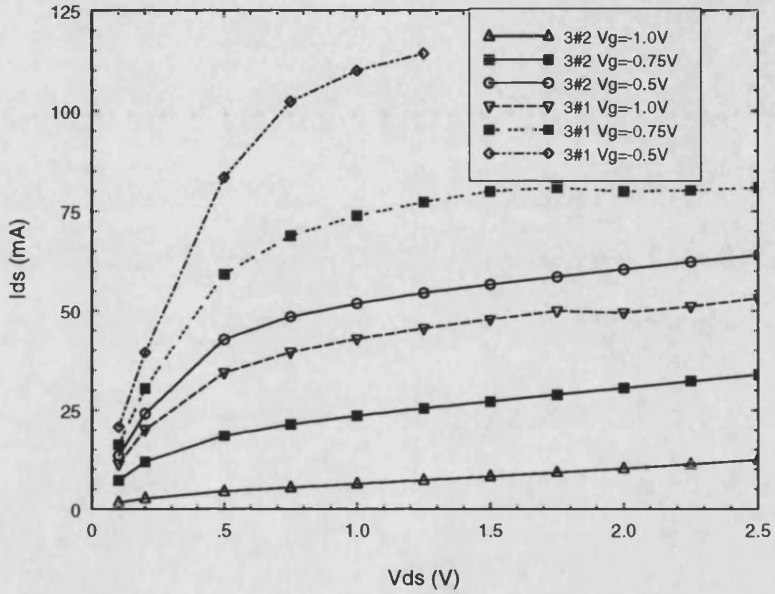

Figure 5.21: Output I-V characteristics for FET 3#1 and FET 3#2

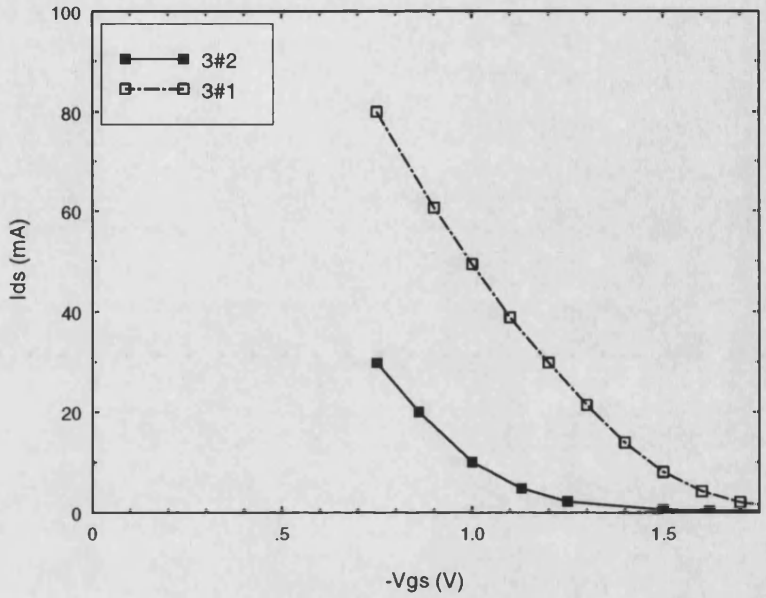

Figure 5.22: Transfer I-V characteristics for FET 3#1 and FET 3#2

A large spread in the d.c. characteristics is again observed as for FET 1 and FET 2. The d.c. parameters are calculated and shown in table 5.2, the transfer results were measured at V_{ds}=2.0V and g_m is calculated at V_{gs}= -1.0V. R_{ds} is calculated at V_{ds}=1.8V and V_{gs}=-0.75V.

	GMMT	FET 1		FET 2		FET 3	
	typ.	1#3	1#7	2#1	2#4	3#1	3#2
I_{dss} (mA)	30 - 60	134	117	148	196	178	98
g_m (mS)	20 - 40	100.8	95.5	113	129	109.6	60.8
R_{ds} (Ω)	640	100	150	272	98	250	294
V_p (V)	-1.8	-1.57	-1.45	-1.75	-1.8	-1.8	-1.8

Table 5.2: D.C. parameters of FET 1, FET 2 and FET 3 compared with GMMT data

The FET 3 device has a total width of 1.36mm, however, since there are only one set of joining vias on the source and drain lines, the active gate length of FET 3 is only slightly less than that of FET 1 which is 1.2mm. The FET 3#1 results for I_{dss} and g_m fall within the ranges specified by the manaufacturer. However, FET 3#2 is below specification for both I_{dss} and g_m, this may be due to the use of active gate widths of 600μm, much wider than the normal foundry standard of 300μm. The channel resistance for both devices does

not agree well with expected trends, this may again be due to the large active gate widths of the FET 3 device. The pinch-off voltage is well within the range specified by GMMT.

These results have shown a large spread in the d.c. parameters of the FET 3 devices, the microwave characterization in the following sections shows that provided the d.c. channel resistance is set at the same level, very similar microwave performance is obtained for the two devices.

5.3.3 Microwave Characterization of FET 3

Introduction

In this section the six-port S-parameters of FET 3#1 and FET 3#2 are measured from 0.1GHz to 20GHz. FET 3#1 is mounted with 56pF d.c. blocks and choke coil biasing. FET 3#2 uses the on-chip gate resistors and d.c. blocks and thus only the source - drain S-parameters are shown in this case.

Measured Results

FET 3 #1 had been mounted in the microwave test fixture shown in figure 4.42, with the high impedance transmission line choke replaced by a choke coil. The source - drain S-parameters are shown below

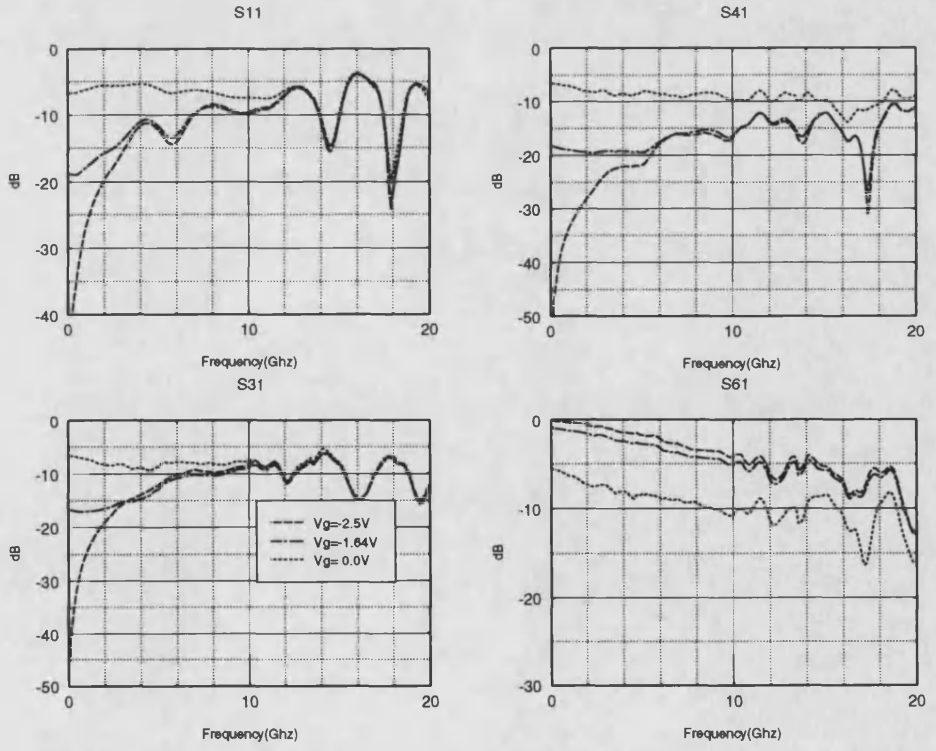

Figure 5.23: Source - drain S-parameters for FET 3#1 with 56pF d.c. blocks and choke coil

The basic trends observed here are the same as for FETs 1 and 2 with backward directional coupling being exhibited in the high channel resistance states. The backward coupling was at a lower level than for FETs 1 and 2, as the basic model had predicted and the through transmission was higher. However, the forward coupling for FET 3 is higher, that is worse, in terms of directivity than for either FET 1 or FET 2, and this for the optimum structure predicted by the basic model. The other feature of these results is the high level of the reflection coefficient in the high resistance states. It was felt that this might be the cause of the poor forward coupling, in that, high reflections from port 3 could produce poor overall forward coupling as discussed earlier. Before investigating this further the gate S-parameters were measured and are shown below

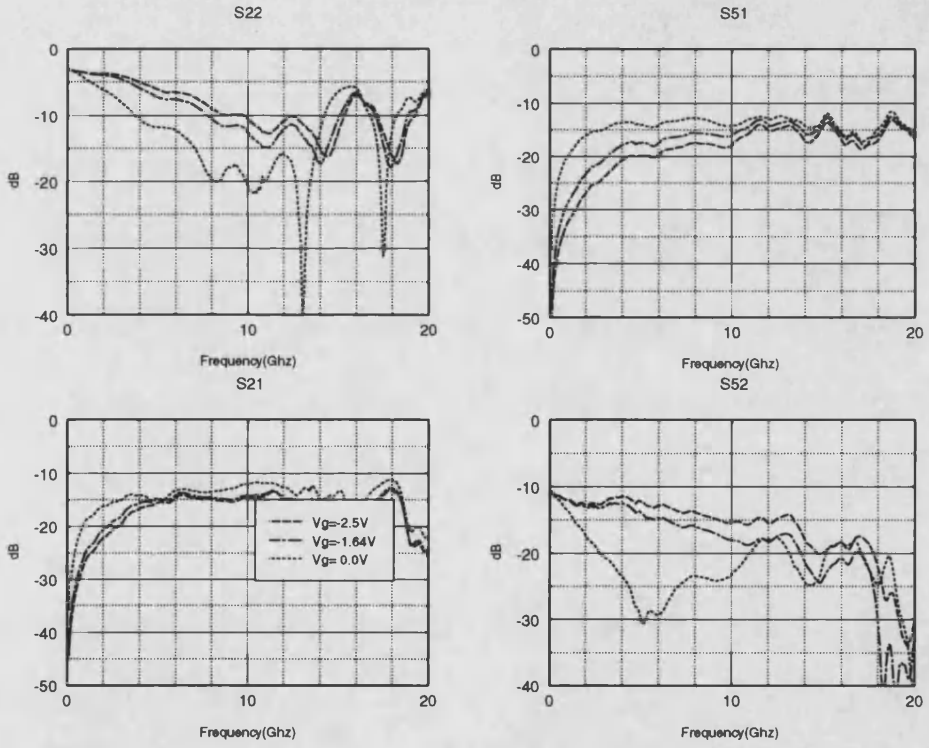

Figure 5.24: Gate S-parameters for FET 3#1 with 56pF d.c. blocks and choke coil

If these are compared to those of FET 2#1 in figure 5.9 similar trends are observed. The through transmission at 0.1GHz is higher for FET 3 than for FET 2 since the devices have the same gate cross section but FET 2 is wider than FET 3, producing a higher series resistance. The difference between forward and backward coupling in the high channel resistance states

is much less than for the other FET structures, this is most likely due to the large difference in electrode lengths, i.e. 94μm : 0.5μm, leading to a reduction in the directional properties of the structure.

Returning to the source - drain S-parameters, the poor reflection coefficient of the source - drain S-parameters was seen as a key feature of these results and reasons for this performance were sought. The first possibility was that the sharp discontinuities joining the source and drain line bond pads to the electrodes where having a much larger effect than expected. As part of the the design of the FET 3 devices a control device was also designed which consisted of only the M3 layer metallization, that is, no gate line, no active layer and no M1 metal layer. Thus measurements on this device would show up any poor performance of the discontinuities alone. These measurements are shown below, the device is denoted COUP 3#1

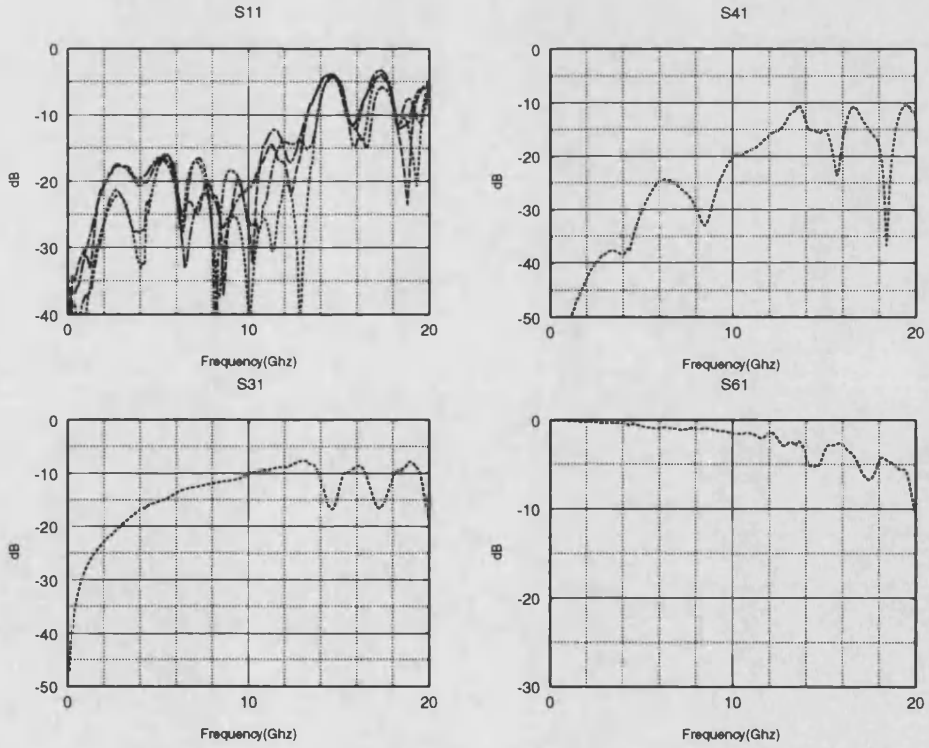

Figure 5.25: S-parameters for COUP 3#1 showing all port reflection coefficients

The form of these results is as expected, showing backward coupling. The through transmis-

sion is much higher than for FET 3#1 and this result shows that the presence of the gate electrode and the resistive nature of the wide FET device adds ≃3dB of loss at 10GHz. The forward coupling is much lower than for the FET 3#1 device as is the reflection coefficient. If the parasitics of the bond pad to electrode transmission lines had been high, these results would have been been much less good. These results imply that the basic model could not predict the performance of the FET 3#1 structure well. As will be seen subsequently, the addition of the electrode resistances to the basic model does not account for the large discrepancies observed. The model required another large effect to be included to model this performance, the next section will outline further improvements in the model which resulted in good model agreement for all three FET structures.

As a repeatability check, to ensure that this performance was not caused by a poor fabricated device, another FET 3 device was mounted and tested. FET 3#2 was mounted in a microwave test fixture and having checked the performance of the on-chip resistor d.c. block combination as being good, it was decided to terminate the gate on-chip. The results are shown below

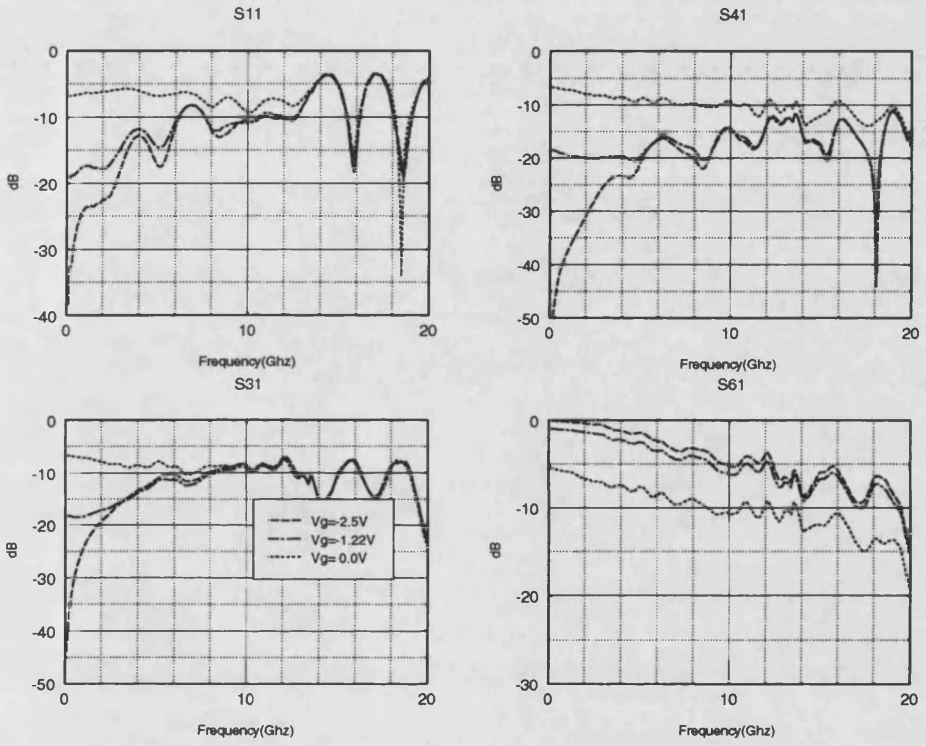

Figure 5.26: Source - drain S-parameters for FET 3#2 with on-chip 36pF d.c. blocks and gate resistors

FET 3#2 shows very similar performance to FET 3#1. The levels at 0.1GHz of the mid bias points are different, this reflects the very different d.c. characteristics of the devices measured earlier. The microwave performance, however, exhibits good repeatability. These measurements implied that the performance of the FET 3 devices was indeed much poorer than expected and further extensions to the model would be required

Conclusions

Two FET 3 devices have been characterized from 0.1GHz to 20GHz, their performance was found to be less good than expected. A passive structure was used as a experimental control to show that the poor performance was not being caused by the sharp discontinuities in the transmission lines connecting bond pads to the source and drain electrodes. The performance of the second device showed good repeatability to the first device, showing that the poor performance was not caused by defects on one particular device. This led to the conclusion that the basic model lacked a major element, this is confirmed in the next section where the performance of the basic model is shown.

5.3.4 Modelling of FET 3

In this section, using the basic model with added electrode resistances, the performance of FET 3 was simulated. The device geometry used for simulation is given below

Source length = 94μm

Drain length = 94μm

Gate length = 1.0μm

Drain to Gate spacing = 2.3μm

Source to Gate spacing = 2.3μm

Device width = 1360μm

As with FET 1 the long source and drain lines result in only one node on the 0.5μm gate line for inter-electrode capacitance calculations, thus a gate length of 1.0μm is used to enable 3 nodes to be placed on the gate.

The resistances of the electrodes were measured, the gate series resistance was found to be, R_g=220Ω, this is a resistance per metre of 161.7KΩ/m, this compares well with the FET 2 gate resistance of 162.5KΩ/m. The source and drain electrode resistances gave a resistance per metre of 225Ω/m, much less than FETs 1 and 2 as expected.

Fitting of the model to measured data was carried out and as expected only a poor fit was obtained. The model predicted much better performance than was obtained, thus the variation of the model data with depletion capacitance is not shown here and only best fitted results are shown. The source - drain S-parameters are shown in figure 5.27

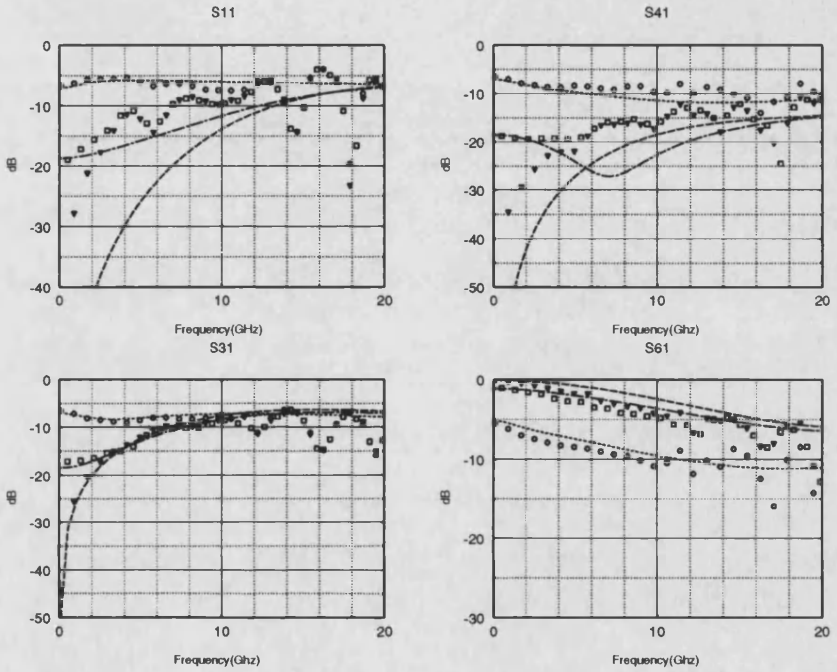

Figure 5.27: Measured and modelled source - drain S-parameters for FET 3

Reasonable fit is obtained for the through transmission, reflection coefficient and backward coupling, however, the forward coupling in the high resistance states is not simulated well. The gate S-parameters were also measured and modelled, the results are shown in figure 5.28

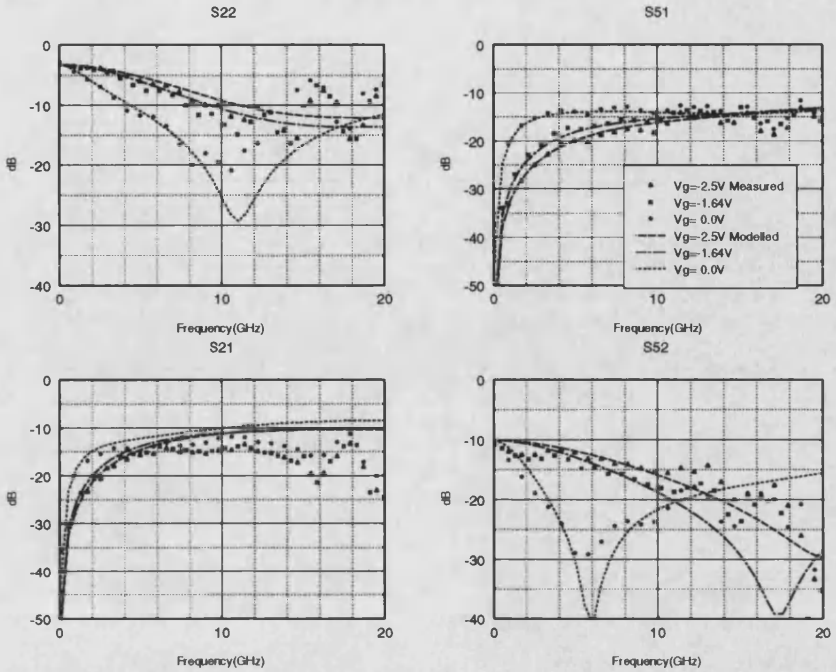

Figure 5.28: Measured and modelled gate S-parameters for FET 3

The fit obtained here is good for all the gate S-parameters, this suggested that the problems in the model lay in the source - drain elements. The final values for the parameters of the model are given below

Depletion Capacitance

$C_{dep(zero\ bias)} = 500pF/m$

$C_{dep(mid\ bias)} = 130pF/m$

$C_{dep(pinch-off)} = 90pF/m$

Channel Resistance

$R_{ds(zero\ bias)} = 5.4m\Omega.m$

$R_{ds(mid\ bias)} = 0.22\Omega.m$

$R_{ds(pinch-off)} = 82\Omega.m$

Electrode Resistance

$R_g = 161.7K\Omega/m$

$R_s = 225\Omega/m$

$R_d = 225\Omega/m$

Depletion Resistance

$R_{dep} = 2.1\Omega.m$

Connection Inductances

L_c=0.3nH

5.3.5 Conclusions

A third wide FET structure has been fully characterized. The electrode geometry was predicted by the basic model as giving good directional coupler performance, this has not been found to be the case. A passive two coupled line structure has been used as a control and found to have reasonable performance, this suggests that the poor performance is not due to the test fixture or the sharp discontinuities used on-chip. Thus it seems that the basic model requires further elements to adequately model this structure, these enhancements are investigated in the next section.

5.4 Final Wide FET Model Improvements

5.4.1 Introduction

In the preceding sections of this chapter it has been seen that the model developed fitted FET 1 reasonably well, FET 2 in general was also modelled well, apart from the forward coupling at pinch-off, however, the forward coupling for FET 3 could not be modelled in either the mid bias or the pinched-off states. This led to an investigation into improvements to the model, these are outlined below.

5.4.2 Ohmic Contact Resistances

In the basic model the ohmic contact resistances have been included in the channel resistance, more strictly these are represented as discrete elements as shown below

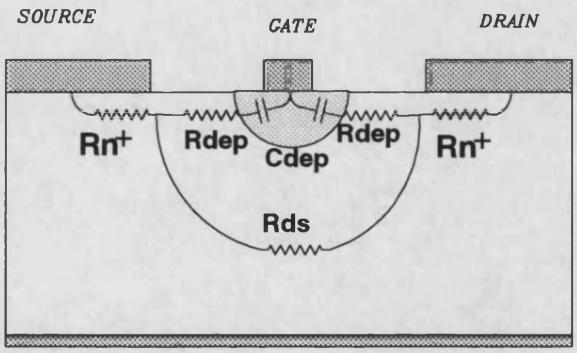

Figure 5.29: FET model with added ohmic contact resistance

The value of the ohmic contact resistance, R_{n+} was set at 2.1mΩ.m using data from the GMMT design manual [24], to maintain the total lumped channel resistance at 4Ω, the zero bias channel resistance was reduced in each case. The S-parameters for the three devices were resimulated using the updated model, the element values used for the three devices are summarized in table 5.3 below, the values of some of the depletion capacitances are different from the optimized values of previous sections, this is to allow comparison of model improvements shown in this section.

	FET 1	FET 2	FET 3
Source/Drain length (μm)	38	22	94
Source/Drain spacing (μm)	2.3	2.3	2.3
Gate length (μm)	1.0	0.5	1.0
Device width (μm)	1500	2000	1360
$C_{dep}(1)$ (pF/m)	600	600	600
$C_{dep}(2)$ (pF/m)	295	200	194
$C_{dep}(3)$ (pF/m)	147	167	167
$R_{ds}(1)$ (mΩ.m)	3.9	5.9	3.4
$R_{ds}(2)$ (Ω.m)	0.24	0.32	0.22
$R_{ds}(3)$ (Ω.m)	90	120	82
R_{dep} (Ω.m)	2.1	2.1	2.1
R_{n+} (Ω.m)	2.1	2.1	2.1
R_g (Ω/m)	103.7K	162.5K	161.7K
$R_{s,d}$ (Ω/m)	733	800	225
L_c (nH)	0.3	0.3	0.3

Table 5.3: Model element values for FET 1, FET 2 and FET 3

Where $C_{dep}(1)$ is the zero bias depletion capacitance, $C_{dep}(2)$ is the mid bias depletion capacitance and $C_{dep}(3)$ is the pinched-off depletion capacitance. The drain - source resistance follows the same convention.

The measured and modelled results for the three devices are shown in figures 5.30- 5.35. The effect of the added ohmic contact resistance was found to be small. These results are not optimized for best fit but are used as benchmarks for comparison with the results of the further improvements to the model discussed in this section. All model parameters shown in table 5.3 will remain constant in this section, so as comparisons can be made when improvements to the model are introduced.

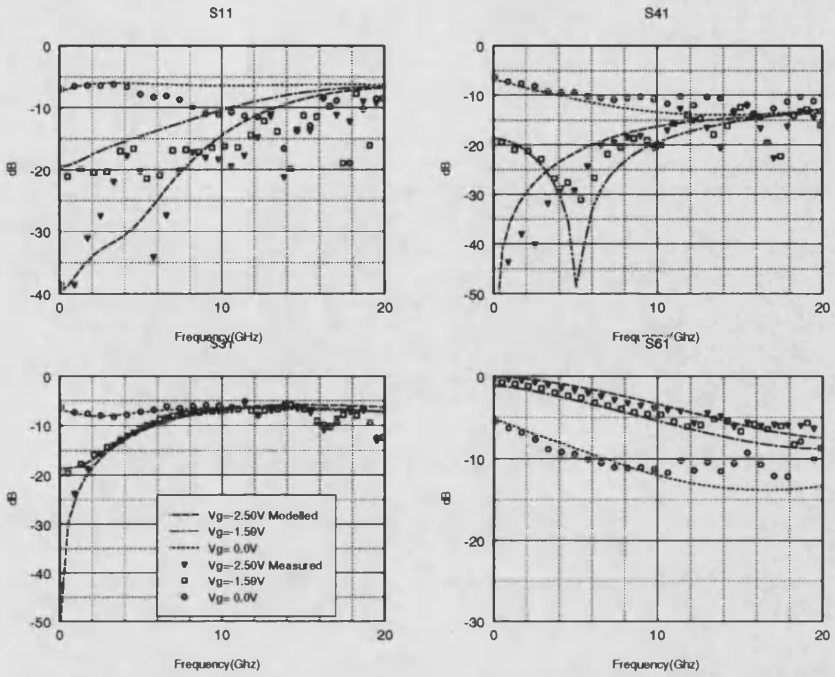

Figure 5.30: Source - drain S-parameters for FET 1 with added ohmic resistance

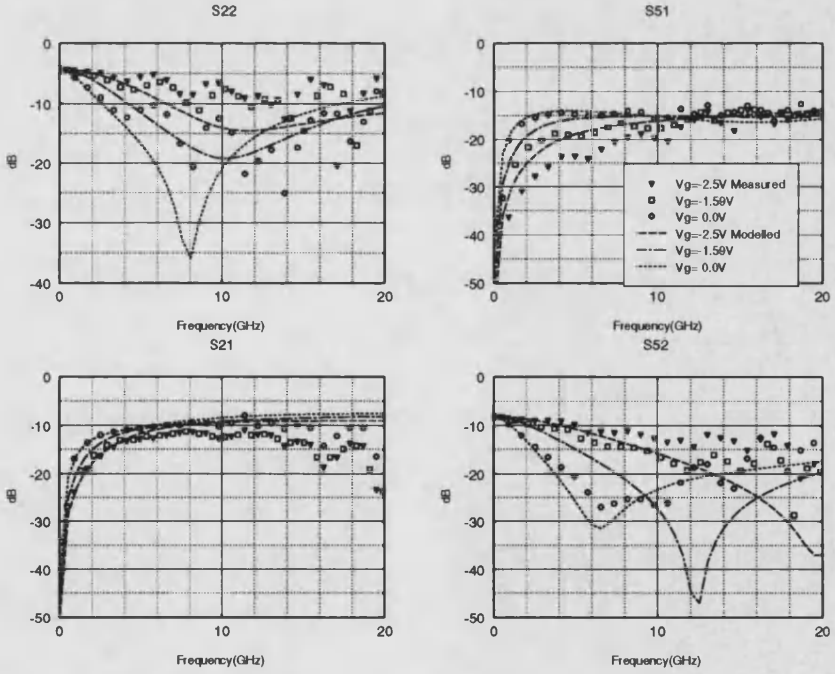

Figure 5.31: Gate S-parameters for FET 1 with added ohmic resistance

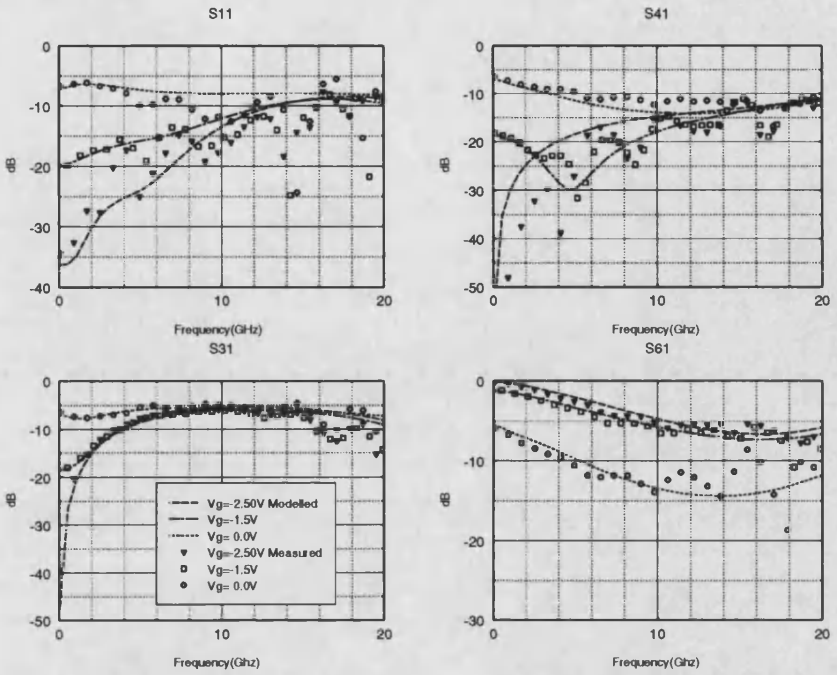

Figure 5.32: Source - drain S-parameters for FET 2 with added ohmic resistance

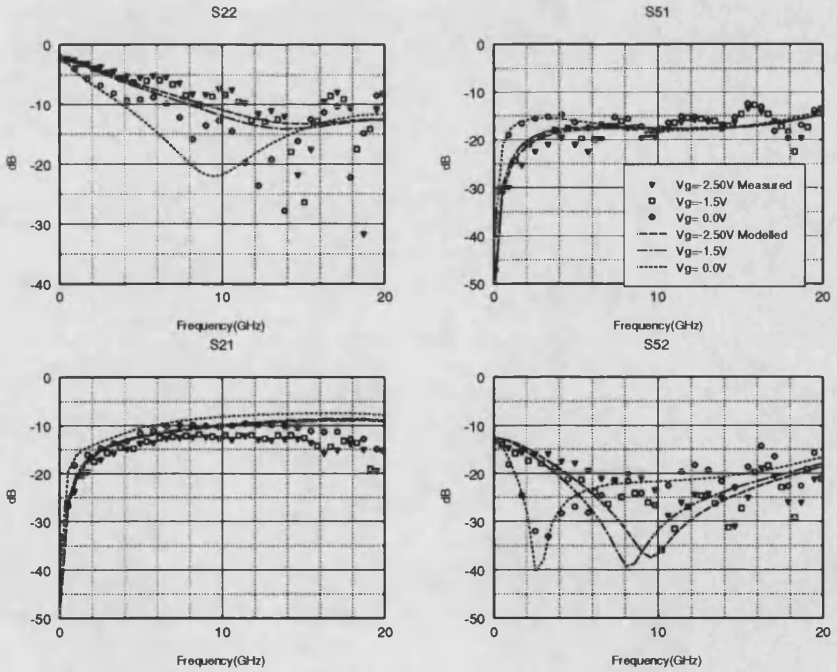

Figure 5.33: Gate S-parameters for FET 2 with added ohmic resistance

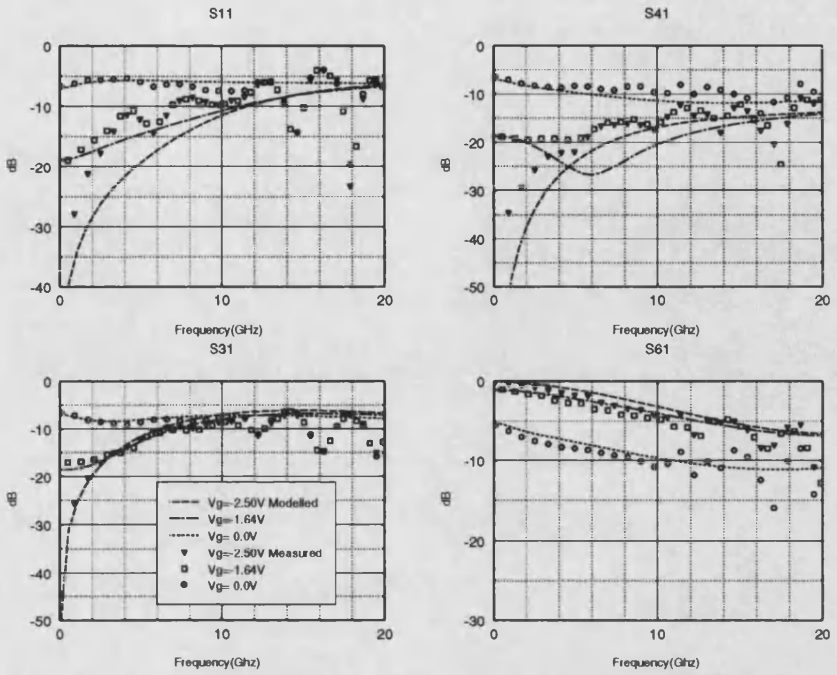

Figure 5.34: Source - drain S-parameters for FET 3 with added ohmic resistance

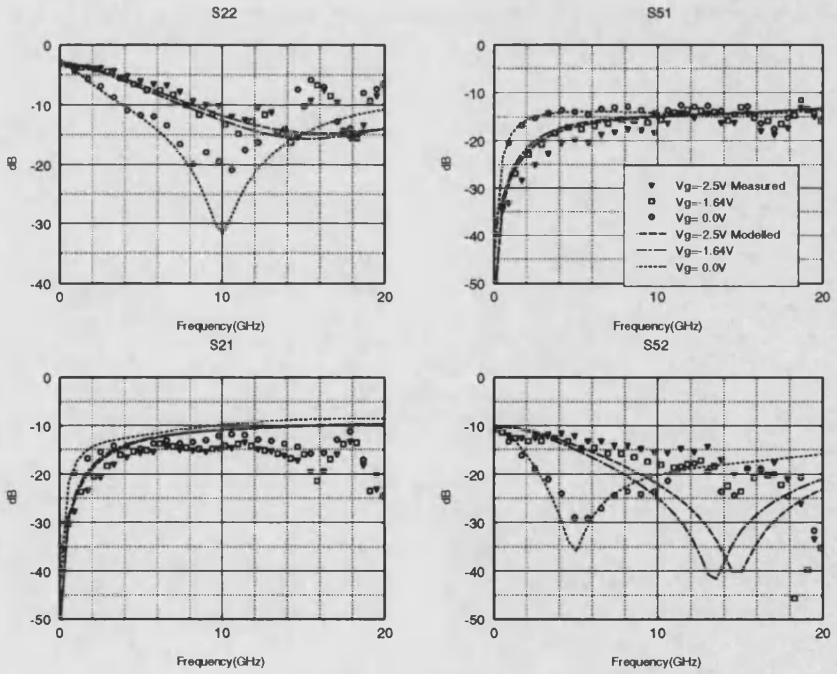

Figure 5.35: Gate S-parameters for FET 3 with added ohmic resistance

5.4.3 Gate Masking

The effect whereby the depletion region of the gate line masks the dielectric path inter-electrode capacitances is introduced to the model in this section. As discussed in chapter 2, only the air-path capacitances are required, these are calculated from the air-filled capacitance matrix and thus this effect is introduced without the need to recalculate the inter-electrode capacitances. The results for the three devices were simulated including gate masking and are shown in figures 5.36- 5.41.

Comparing the source - drain S-parameters of the three devices with and without gate masking, it is seen that generally only small differences occur. In the case of FETs 1 and 2 the mid bias forward coupling shows the largest change, with a reduction in the Q of the resonance. The pinched-off forward coupling shows no change. In FET 3 the resonant frequency of the mid bias forward coupling is shifted up in frequency and the pinched-off response is reduced by 2-3dB.

However, the major effects are observed on the gate S-parameters, this is as expected since it is the gate inter-electrode capacitances that are altered by the gate masking effect. For all three devices the fit is dramatically improved, especially in the through transmission and forward coupling. The resonances in the through transmission without gate masking are moved up in frequency in the mid bias and pinched-off states, this is similar to the trend observed in the model optimizations shown previous sections where reductions in the depletion capacitance increased the through transmission resonant frequency.

These measurements show that the gate masking effect is a substantial effect and must be included in any quasi-TEM model of a wide FET structure.

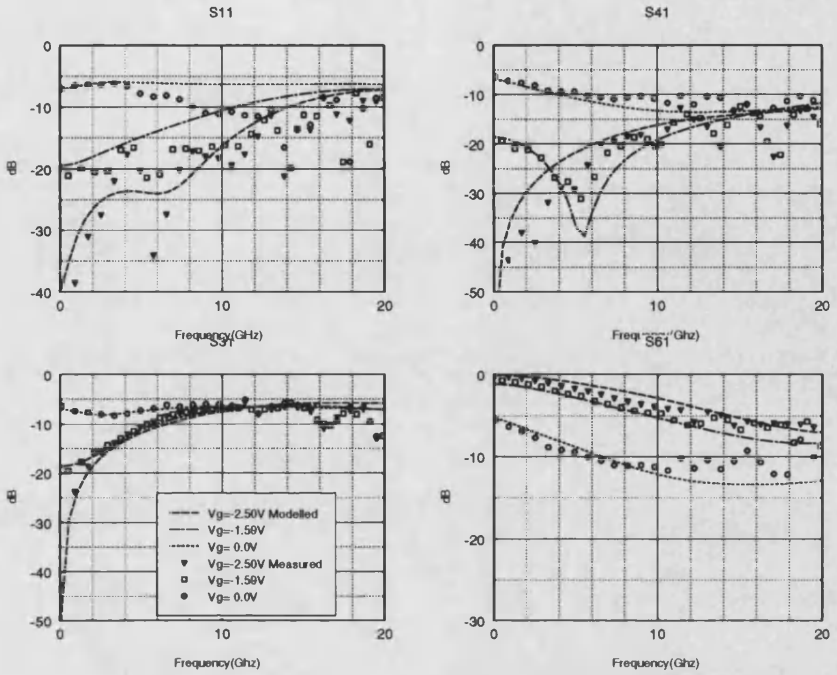

Figure 5.36: Source - drain S-parameters for FET 1 with added ohmic resistance and gate masking

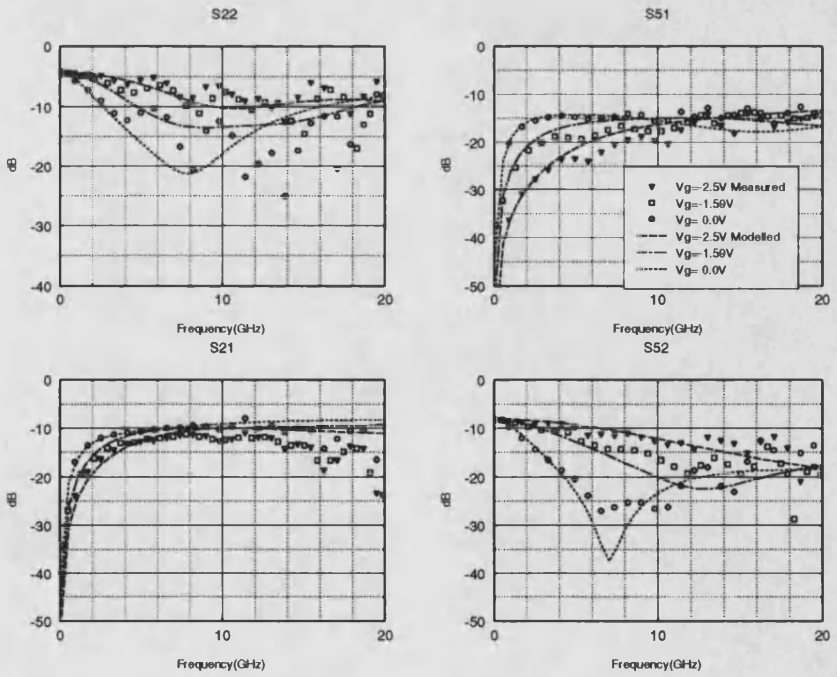

Figure 5.37: Gate S-parameters for FET 1 with added ohmic resistance and gate masking

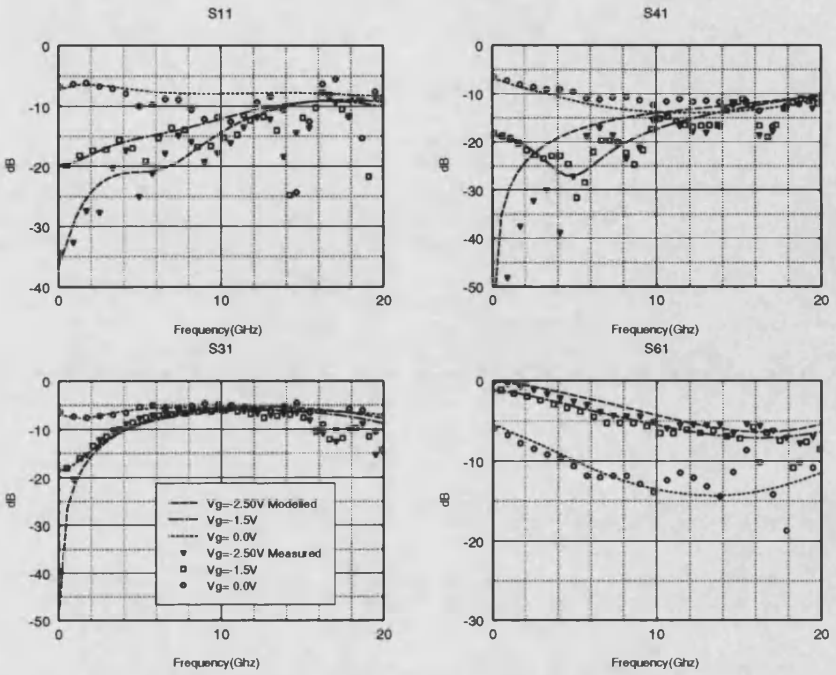

Figure 5.38: Source - drain S-parameters for FET 2 with added ohmic resistance and gate masking

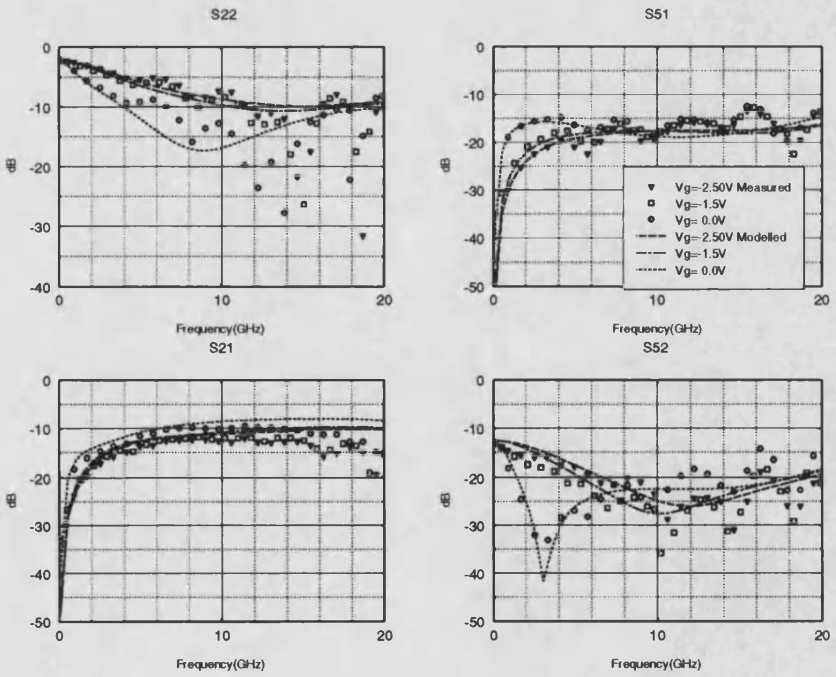

Figure 5.39: Gate S-parameters for FET 2 with added ohmic resistance and gate masking

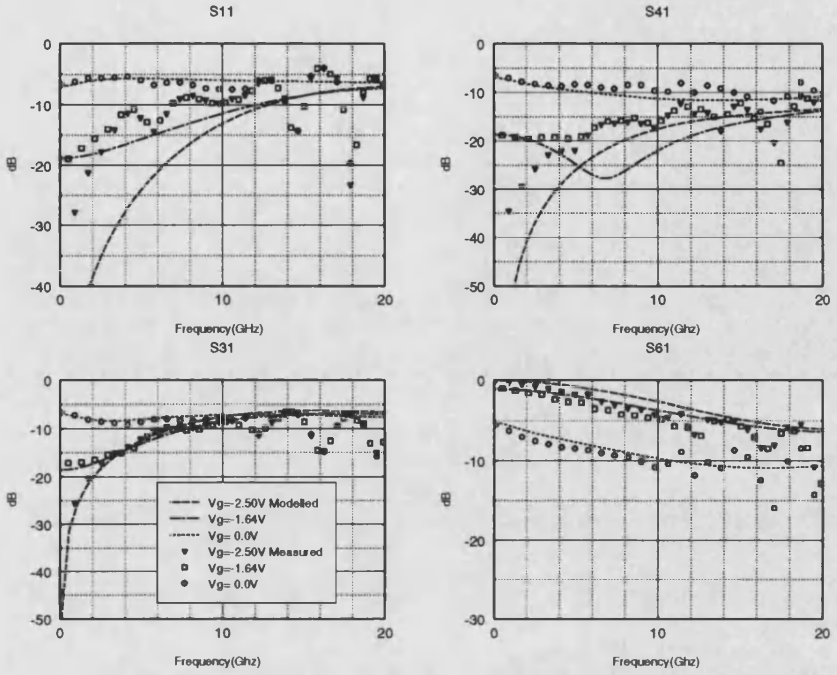

Figure 5.40: Source - drain S-parameters for FET 3 with added ohmic resistance and gate masking

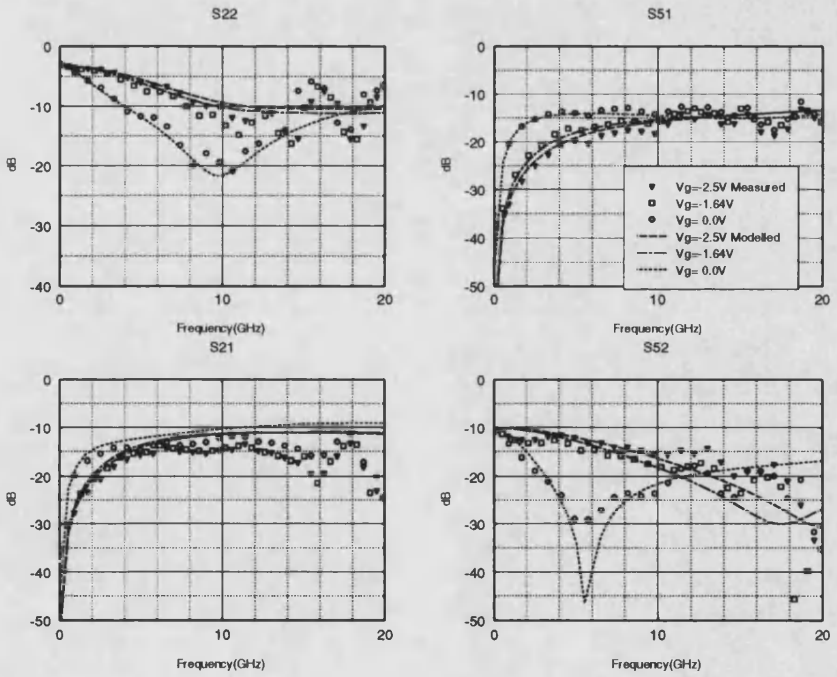

Figure 5.41: Gate S-parameters for FET 3 with added ohmic resistance and gate masking

5.4.4 Finite Thickness FET Electrodes

As an attempt to investigate the effect of the inter-electrode capacitances on the final S-parameters of the structure, the capacitance values were varied manually. It was found that increasing drain - source inter-electrode capacitance resulted in higher forward coupling at pinch-off in the FET 3 case, improving the fit of the model, and in the case of the FET 2 device, resulted in a decrease in the forward coupling at pinch-off, also an improvement in the fit of the model. Thus it seemed that the estimate of the source - drain capacitance was too low and reasons for this were sought.

One of the assumptions made for the calculation of the inter-electrode capacitances was that the electrodes were infinitely thin, in chapter 2 it is seen that this is not the case. The finite thickness of the source and drain electrodes would produce a larger drain - source capacitance and thus could improve the fit of the model.

Using the resistive network analogue technique extended to finite thickness lines, the inter-electrode capacitances were calculated for the FET structures with source and drain lines of thickness 3μm and zero thickness for the gate line. However, as discussed in chapter 2, these results required the use of substantially less nodes across the FET electrodes, it was felt this may well reduce the accuracy of the calculated capacitances. This seemed to be the case since for thick lines, it was found that the drain - source capacitance, for certain structures was in fact less than the zero thickness case, which seemed intuitively incorrect. For the FET 2 structure, the source - drain capacitances were found to be larger as expected, in the dielectric filled and air filled cases increases of 10% and 50%, respectively were found. The effect on the device S-parameters is shown overleaf

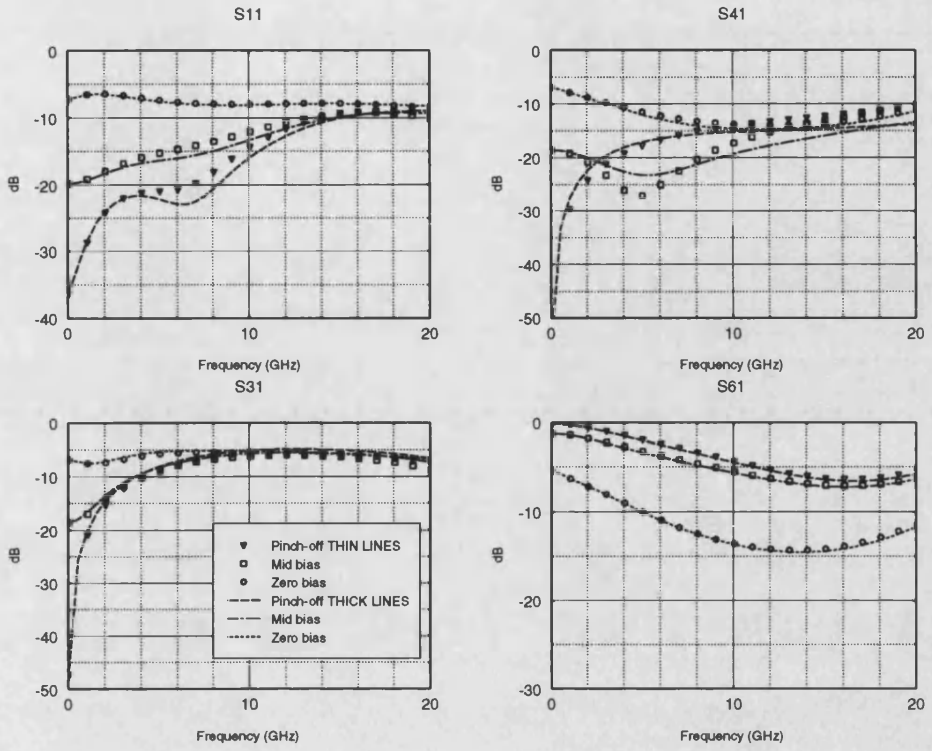

Figure 5.42: Comparison of source - drain S-parameters for FET 2 with 3.0μm and zero thickness source and drain electrodes

Only the forward coupling shows any substantial differences, the pinched-off response is seen to be slightly higher for thick lines, the opposite to the effect required. It seems that the increase in the dielectric filled source - drain capacitance is not large enough to reduce the forward coupling at pinch-off and in fact the response may well be dominated by the large change in the air filled source - drain capacitance, from which the mutual source - drain inductance of the structure is calculated. It was felt that finite thickness inter-electrode capacitances could not be calculated with the same accuracy as in the zero thickness case and moreover the above results suggest that the the effect produced is not large enough to improve the fit of modelled to measured data. Thus, other, larger effects were sought that might increase the source - drain capacitance.

5.4.5 FET Intrinsic Source - Drain Capacitance

The basic model developed in chapter 2 assumed that the intrinsic source - drain capacitance of the FET was adequately modelled by the dielectric path source - drain inter-electrode capacitance. However, the presence of the highly doped ohmic contact regions beneath the source and drain lines effectively extends the source and drain contacts and brings them into close proximity [38]. There is thus an extra capacitance associated with the ohmic contact regions. This seemed like the effect that was required to improve the fit of the wide FET model since this would only increase the source - drain inter-electrode capacitance and not affect any of the other inter-electrode capacitances or inductances. This extra capacitance, termed C_{ds} was added to the model in parallel with the channel resistance, R_{ds} as shown below

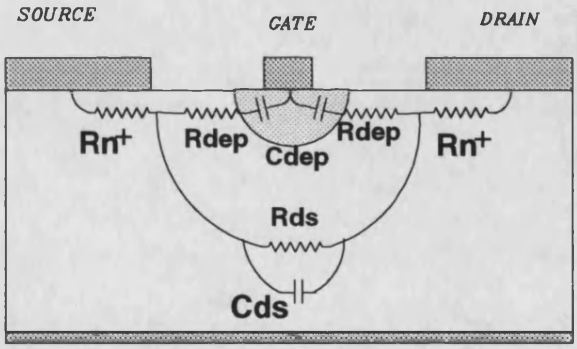

Figure 5.43: FET model with added ohmic contact resistance and C_{ds} component

The results for the three devices were resimulated, the value for C_{ds} was obtained by fitting modelled to measured data, the final parameter values are shown in table 5.4

	FET 1	FET 2	FET 3
Source/Drain length (μm)	38	22	94
Source/Drain spacing (μm)	2.3	2.3	2.3
Gate length (μm)	1.0	0.5	1.0
Device width (μm)	1500	2000	1360
$C_{dep}(1)$ (pF/m)	600	600	600
$C_{dep}(2)$ (pF/m)	295	200	194
$C_{dep}(3)$ (pF/m)	147	167	167
$R_{ds}(1)$ (mΩ.m)	3.9	5.9	3.4
$R_{ds}(2)$ (Ω.m)	.24	.32	.22
$R_{ds}(3)$ (Ω.m)	90	120	82
C_{ds} (pF/m)	50	80	80
R_{dep} (mΩ.m)	2.1	2.1	2.1
R_{n+} (mΩ.m)	2.1	2.1	2.1
R_g (Ω/m)	103.7K	162.5K	161.7K
$R_{s,d}$ (Ω/m)	733	800	225
L_c (nH)	0.3	0.3	0.3

Table 5.4: Final model element values for FET 1, FET 2 and FET 3 including C_{ds}

The measured and modelled results are shown in figures 5.44- 5.49. In all cases the fit of the source - drain S-parameters is improved. The gate S-parameters are unaffected as expected since C_{ds} does not affect the gate associated Y-parameters calculations as discussed in chapter 2.

The forward coupling is the most affected by the introduction of C_{ds}, as anticipated the forward coupling of FET 3 at pinch-off is increased and is decreased for FET 2. For the mid bias state the opposite occurs and the Q of the FET 2 resonance is increased and decreased for FET 3, this maintains a reasonable fit for FET 2 and dramatically improves the fit for FET 3. FET 1 also shows improved fit, the forward coupling at pinch-off has decreased and the Q of the mid bias resonance slightly decreased.

The backward coupling is also affected by the addition of C_{ds}, for all three devices, the level is increased by 2dB-3dB in the low frequency region, <12GHz. This agrees with simple two line theory, in that the addition of C_{ds} will increase the odd mode capacitance of the structure and thus reduce the odd mode impedance and remembering the expression for backward coupling, K_c [37], shown below

$$K_c = \frac{Z_{oe} - Z_{oo}}{Z_{oe} + Z_{oo}} \tag{5.1}$$

Where Z_{oe} and Z_{oo} are the even and odd mode impedances respectively. It is seen that a decrease in the odd mode impedance will increase the backward coupling as observed in the modelled results.

The optimized values for C_{ds} are seen to be the same for FETs 2 and 3 at 80 pF/m and lower for FET 1 at 50 pF/m. This reflects that FET 1 was fabricated using the GMMT F14 process whereas FETs 2 and 3 used the F20 process with a shorter gate length, leading to increased C_{ds} since the ohmic regions would be in closer proximity. In fact it is found [81] that the F20 process has ohmic contact regions that are closer to the gate line than the F14 process in order to reduce the bulk active layer resistances, this would further increase the C_{ds} component.

Thus it is seen that the addition of an extra source - drain capacitance component associated with the proximity of the ohmic contact regions improves the fit of all three wide FET structures. The level of C_{ds} is higher for the F20 designed devices and this reflects the fact that for the F20 process the gate length is shorter and the ohmic contact regions extend closer to the gate line. The model can now be used to predict the performance of these devices with reduced inductive connections which would reflect the level of parasitics present if the device was fully integrated on-chip, the next section will present these results.

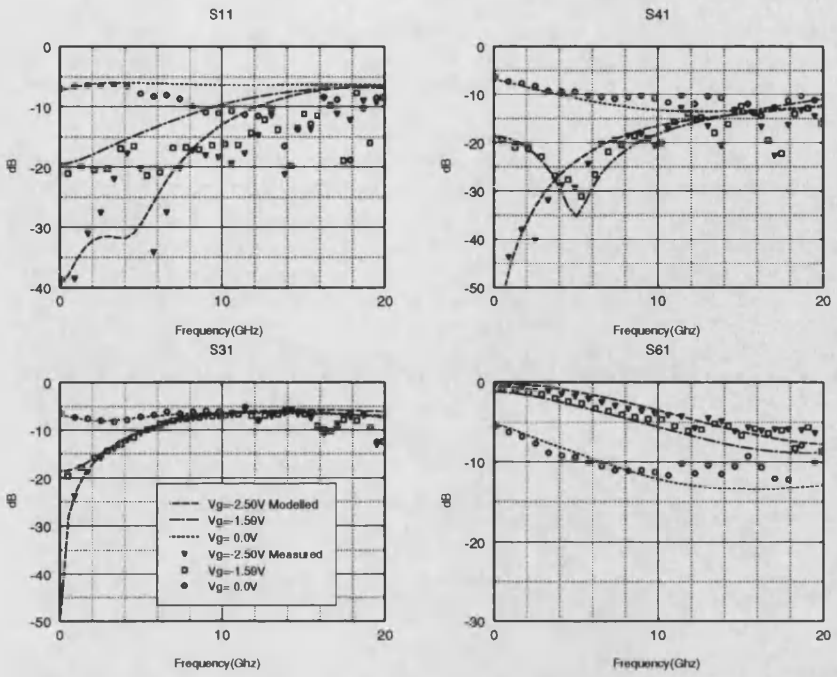

Figure 5.44: Source - drain S-parameters for FET 1 with added ohmic resistance, gate masking and added C_{ds}

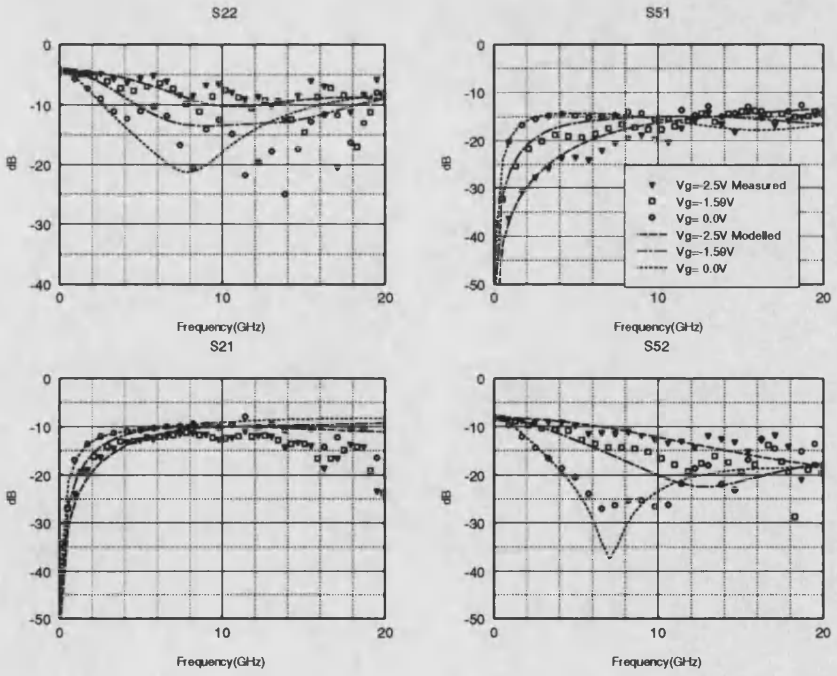

Figure 5.45: Gate S-parameters for FET 1 with added ohmic resistance, gate masking and added C_{ds}

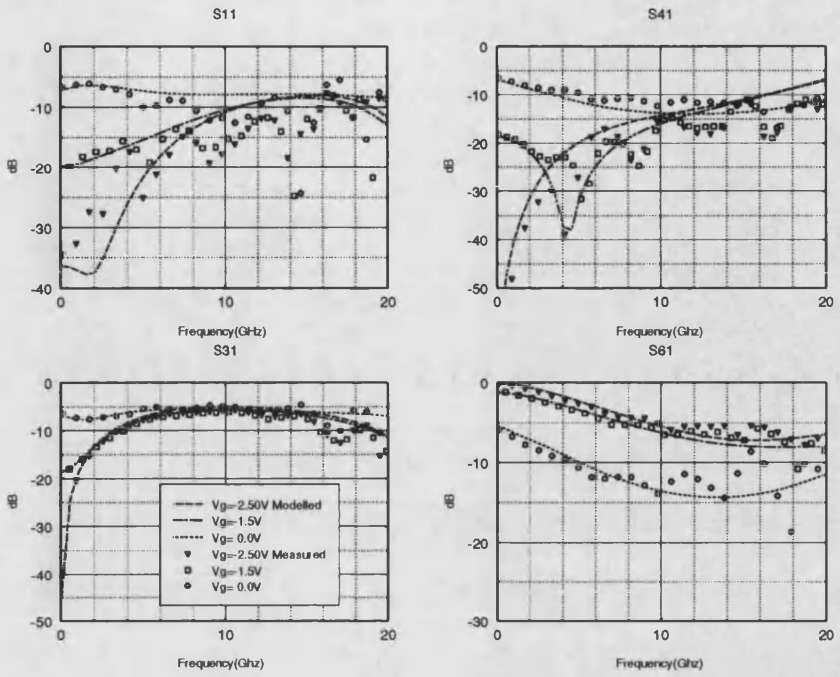

Figure 5.46: Source - drain S-parameters for FET 2 with added ohmic resistance, gate masking and added C_{ds}

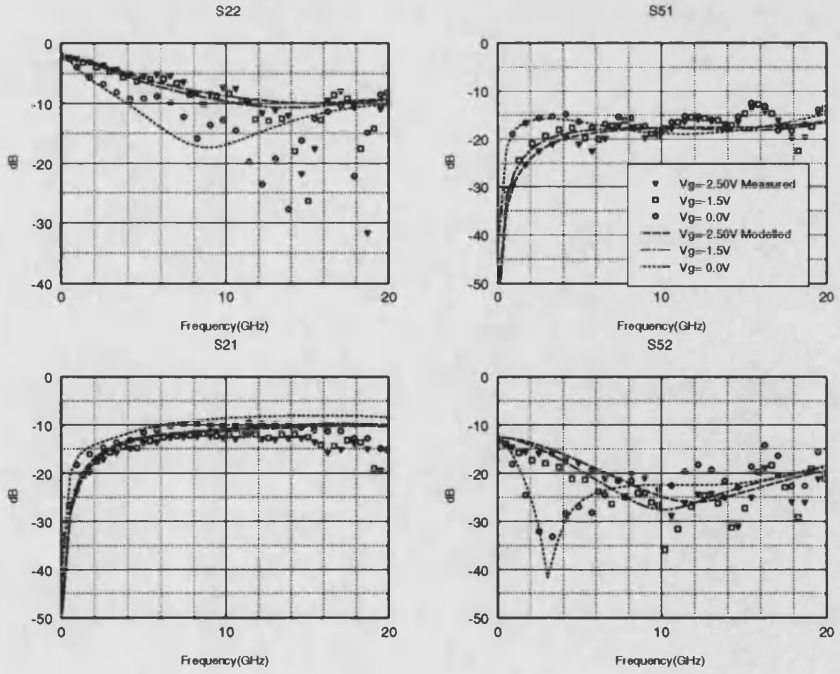

Figure 5.47: Gate S-parameters for FET 2 with added ohmic resistance, gate masking and added C_{ds}

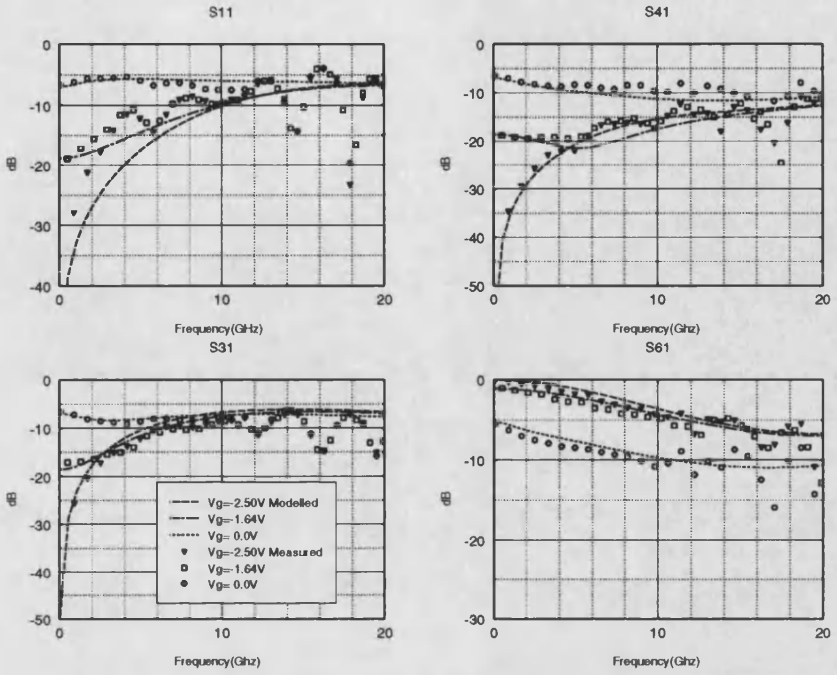

Figure 5.48: Source - drain S-parameters for FET 3 with added ohmic resistance, gate masking and added C_{ds}

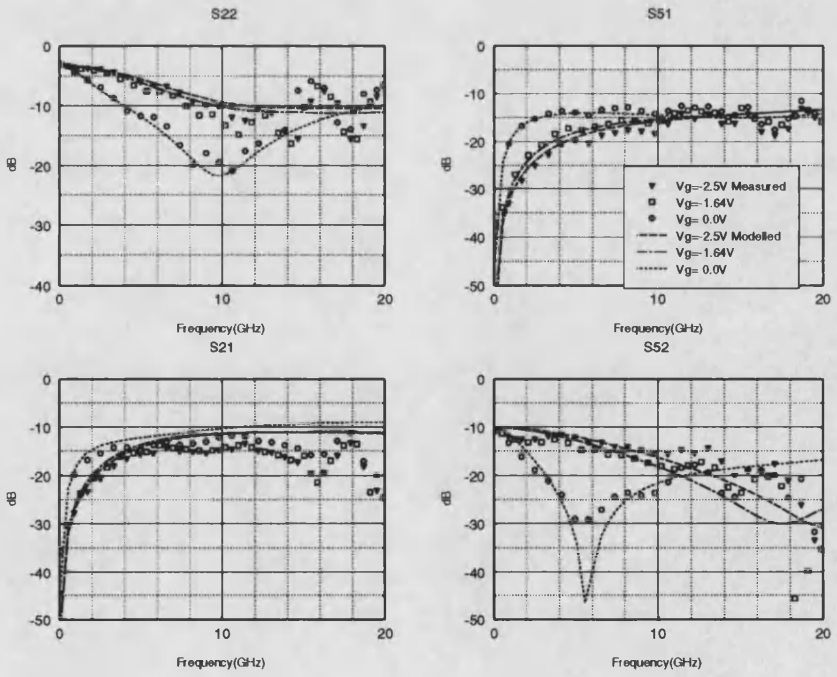

Figure 5.49: Gate S-parameters for FET 3 with added ohmic resistance, gate masking and added C_{ds}

5.4.6 Intrinsic Device Performance

Having obtained a model which fits the measured data reasonably well for three different wide FET structures, the effect of the inductive connections to the device can be reduced to levels that could be achieved if the device was integrated on-chip within a system or if high quality on-chip 50Ω loads were used to terminate one of the four ports of the device allowing the intrinsic directivity to be measured. The level of connection inductance was reduced to 0.05nH and the devices were resimulated, only source - drain S-parameters are discussed here, since only these are required to investigate the performance of the device as a variable directional coupler. The results for the three devices are shown below

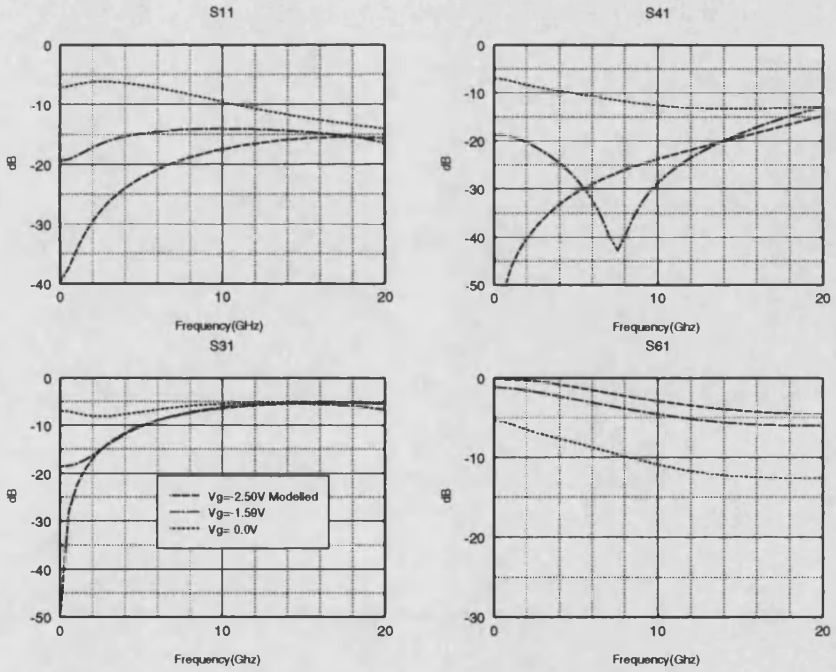

Figure 5.50: Source - drain S-parameters for FET 1 with connection inductances, L_c=0.05nH

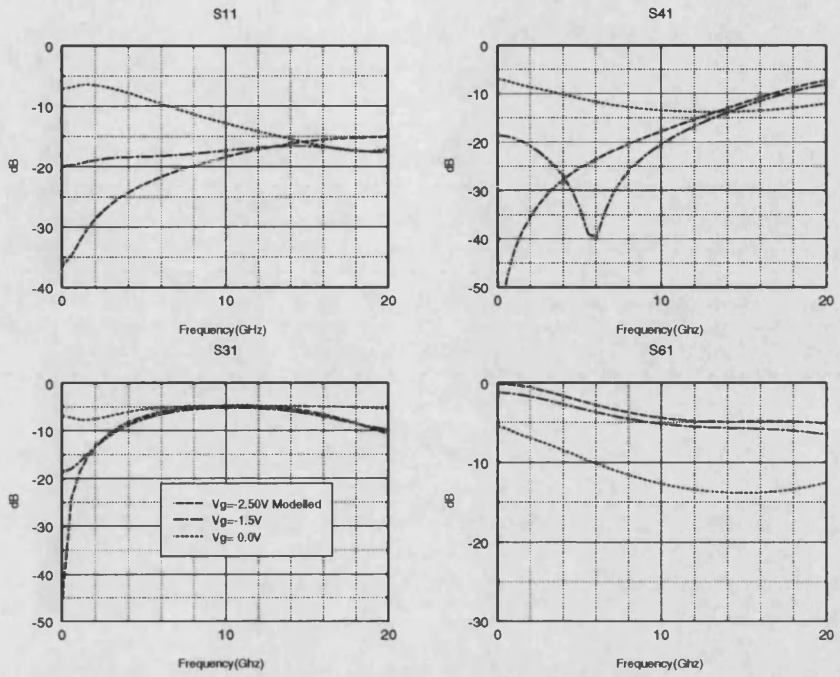

Figure 5.51: Source - drain S-parameters for FET 2 with connection inductances, L_c=0.05nH

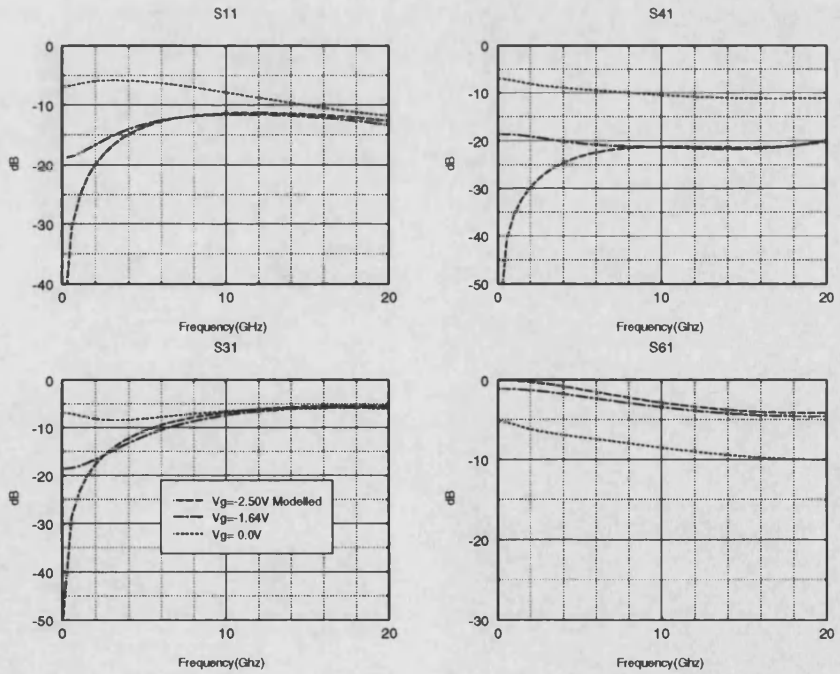

Figure 5.52: Source - drain S-parameters for FET 3 with connection inductances, L_c=0.05nH

In all three cases the forward coupling has reduced as expected, leading to improved directivity. The backward coupling and through transmission are relatively unaffected and the reflection coefficient is reduced at high frequency. Of the three devices FET 1 exhibits the best directivity performance, for comparison with earlier measured data the directivity and coupling were calculated and are shown below at three simulated bias points.

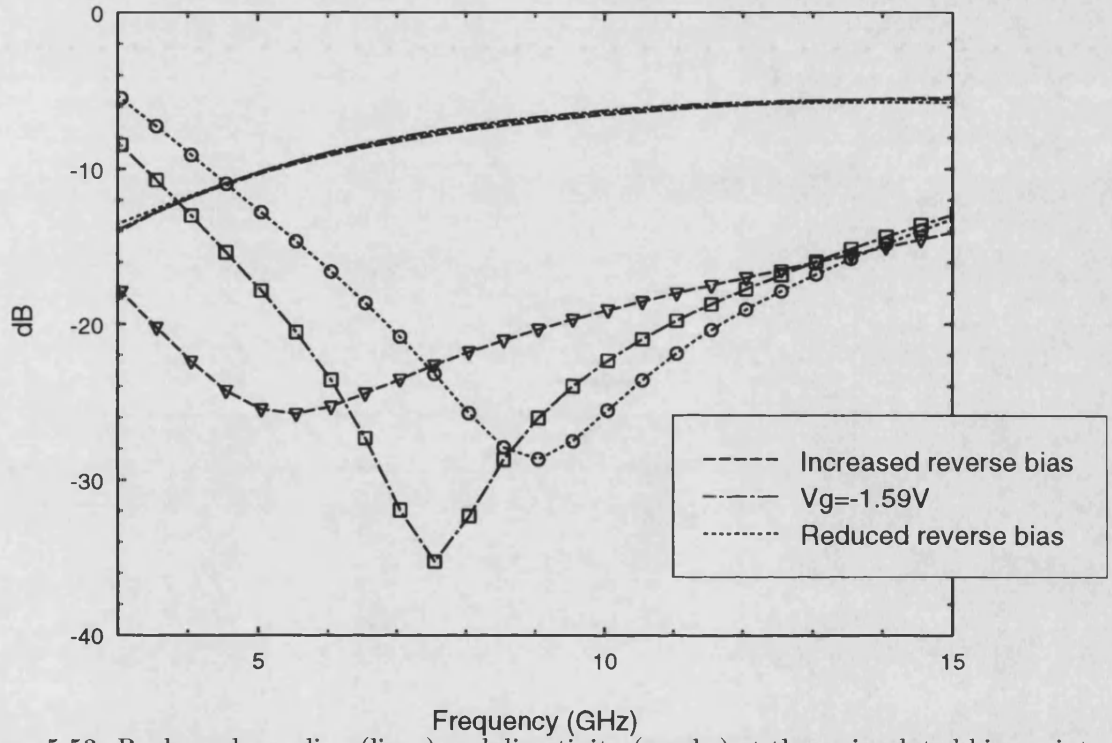

Figure 5.53: Backward coupling (lines) and directivity (marks) at three simulated bias points for FET 1 with L_c=0.05nH

These results show very good directional coupler performance, at V_g=-1.59V the directivity is better than 20dB from 5.5GHz to 10.9GHz with a nominal coupling value of -7.9dB at a flatness of ±1.75dB and the directivity is greater than 30dB over a narrower band, 6.9GHz to 8.3GHz. The results also show the large amount of tunability that can be obtained with these devices, the maximum directivity point can be tuned from 5.0GHz to 9.0GHz. The reflection coefficient and through transmission across this band are shown overleaf

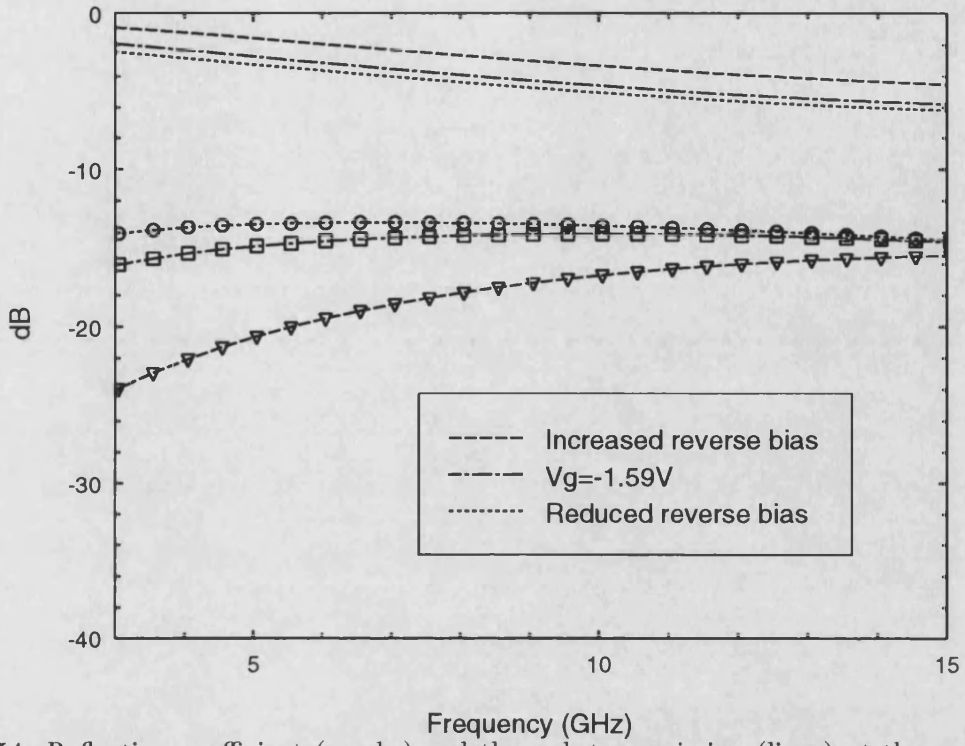

Figure 5.54: Reflection coefficient (marks) and through transmission (lines) at three simulated bias points for FET 1 with L_c=0.05nH

The reflection coefficient is reasonable across the band, the through transmission is lower than would be desired in practical applications, it is hoped that using the model developed this could be reduced to more realistic levels, possible solutions to the low through transmission problem are discussed in the chapter 6 : Further Wide FET Applications.

5.4.7 Conclusions

In this section the basic model has been enhanced by the addition of gate masking and extra source - drain capacitance, the model has been fitted to measured data for three different wide FET structures and a reasonably good level of fit has been obtained for both source - drain S-parameters and gate S-parameters. The performance of the devices with reduced connection parasitics has been simulated using the model and as expected improved performance was predicted. The best performance was obtained for the FET 1 device and the directivity of the device has been shown to be very good across a wide band, but moreover, the directivity can be tuned across a large bandwidth, allowing for example more accurate return loss measurements to be performed at a particular frequency of interest.

5.5 Summary

In this chapter two wide FET devices have been shown in a novel configuration, as six-ports, where the source gate and drain lines are considered as three coupled microstrip transmission lines. It has been found that the forward coupling, and hence the directivity between the source and drain lines can be controlled by the d.c. bias applied to the gate line.

The two devices, with different electrode geometries have been fully characterized both at d.c. and microwave frequencies from 0.1GHz to 20GHz. The measured data has been used to validate the model developed in chapter 2, and is compared with the results from chapter 4 for the FET 1 device. The final, improved model gives good agreement between measured and modelled data for all three devices, at three different gate bias levels and for frequencies from 0.1GHz to 20GHz.

The model was then used to predict the performance of the devices with much reduced parasitics, which would be more representative of those present if the device was integrated on-chip within a system or if on-chip terminations were implemented to reduce internal reflections which tend to degrade the performance of directional couplers. The simulations showed that much improved performance could be obtained, as expected. The model predicted greater than 20dB directivity across a bandwidth of 5.7GHz, centred at 6.3GHz. In addition the frequency of optimum directivity can be tuned across a 4.0GHz band from 5.0GHz to 9.0GHz. The model can now be used to design directional couplers with optimum performance across a particular band and investigate whether changes in the physical structure beneath the FET electrodes, in terms of geometry and doping levels could improve the performance of these devices.

Such devices could have many applications including variable directivity couplers, variable power dividers or combiners and variable phase shifters. Phase shifting applications are investigated in the next chapter. The great advantage of these devices is that they bring on-chip tunability to normally passive structures, giving enormous flexibility to the MMIC

designer who is often restricted by the need for "first-pass" success. These devices show the potential for innovation that the MMIC design process offers, instead of merely transferring standard hybrid microwave technology to monolithic form, traditional microwave techniques can be combined with semiconductor technology to offer completely new types of devices.

Chapter 6

Further Wide FET Applications

6.1 Introduction

In chapters 4 and 5 a wide FET structure has been shown to have useful properties as a voltage controlled directional coupler. In this chapter other configurations are investigated that use the wide FET as a basic element.

Firstly, variable phase shifters are investigated, where source and drain lines are shorted together to form a coupled meandered section of line. This forms one part of a differential Schiffman phase shifter [106], where broadband fixed phase shifts are obtained. By using the on-chip tunability of the wide FET, useful variable phase shifter performance is obtained.

Secondly, two wide FETs are connected in a tandem [107] arrangement such that much higher backward coupling levels are obtained. For certain configurations it is found that the backward coupling is in fact higher than the through transmission, thus enabling the backward coupled port to be used as the through transmitted port. In this configuration higher effective through transmission is obtained than for a single wide FET. Thus improving the one coupler parameter that did not exhibit good performance in the single wide FET case. The voltage variable characteristics are however, somewhat different.

These two examples illustrate the large number of applications that a tunable coupled line structure such as the wide FET could have. This chapter will present measured and modelled results using the model developed in chapters 2, 4 and 5.

6.2 A Variable Phase Shifter Using a Wide FET Structure

6.2.1 Introduction

The use of meandered line sections to introduce extra phase length is well known. If the meandered sections are brought into close proximity a coupled line section is formed and the phase shift of this element is no longer linear with frequency [106]. Schiffman [106] presented measured and modelled results for a differential fixed 90^o phase shifter, constructed from a coupled line section shorted at one end and a non-coupled meandered section. The differential phase shift is obtained by splitting the input power, half to a linear phase shift element and half to the non-linear Schiffman element, this results in a constant differential phase shift over a broad band that can be designed at any phase shift level. The use of this type of phase shifter has continued [108, 109] and remains an efficient method for producing broadband constant phase shift.

In this work the model developed for a wide FET was used to investigate Schiffman section configurations, reasonably large phase shifts were predicted. A number of wide FET structures were then configured as Schiffman sections, measured data will be presented here. Finally, the phase shift of a wide FET Schiffman section was compared to that of an ideal transmission line and relatively constant differential phase shift was obtained across a wide band.

6.2.2 Modelled Results

Using the multiport connection method [79] the source and drain lines of the wide FET model of FET 1 were shorted together, this results in a two-port circuit, the gate line was terminated in 50Ω loads the results are shown below

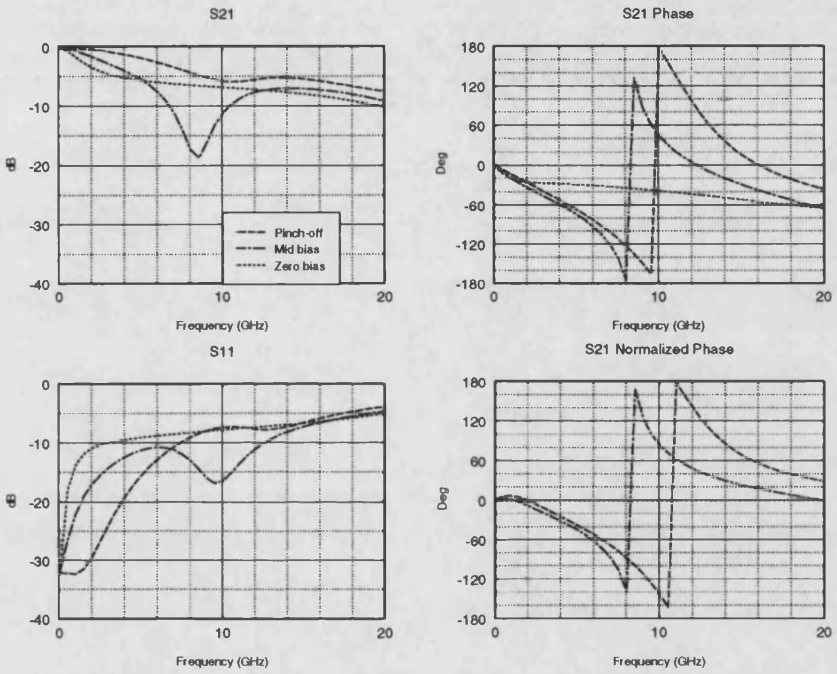

Figure 6.1: Modelled results for FET 1 configured as a Schiffman phase shifter

The results show the modelled through transmission, S_{21}, the reflection coefficient, the through phase shift and the through phase shift normalized to the zero bias state. The model used here does not include gate masking or extra C_{ds} effects and detailed fitting of measured to modelled data has not been carried out, this could be the subject of future work. The wide FET has two states of operation : (i) at low bias levels the channel resistance is low and the phase shift through this resistive path is consequently low, (ii) at high channel resistance the device acts as two coupled lines and a large phase shift is produced. As the device passes between these states a resonance region is passed through, this limits the usable phase shift bandwidth. This resonant behaviour is observed in passive coupled lines and it appears to be related to the length of the coupled region as will become apparent

from subsequent measurements.

These results show that large variations in phase are achievable in this configuration and the non-linear nature of the phase variation could be used to obtained constant differential phase shift. A number of wide FETs were mounted in this configuration and measurements performed, these are detailed in the next section.

6.2.3 Measured Results

Having predicted phase shifter operation using the wide FET model a number of devices were measured. The wide FETs were mounted in the same test fixture as for directional coupler measurements, the set up is shown below

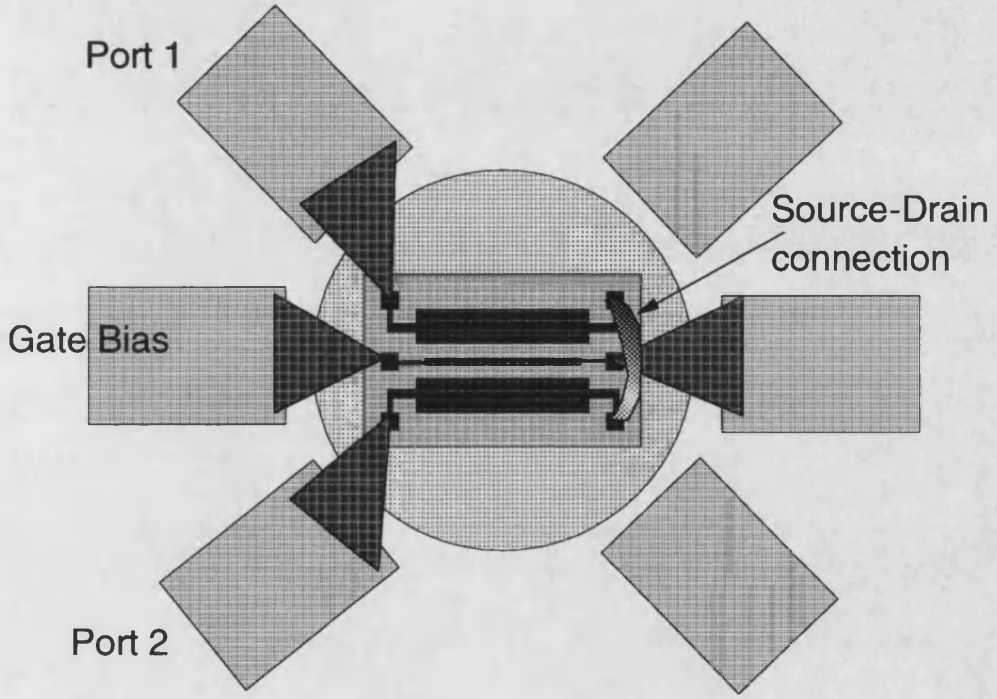

Figure 6.2: Detail of wide FET test fixture for phase shifting applications

Figure 6.2 shows the tape bond from source to drain line and the input and output microstrip lines. The gate line is terminated with 56pF capacitors and coaxial 50Ω loads. The measured results for this configuration are shown in figure 6.3

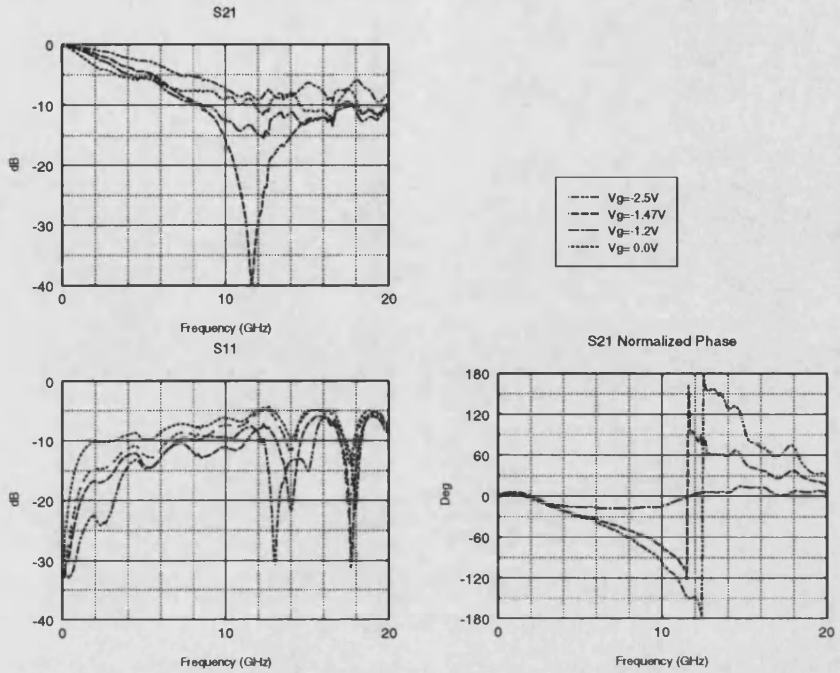

Figure 6.3: Measured results for FET 1 Schiffman phase shifter

These results show similar trends to those predicted by the model. The resonant frequency is different, as is the frequency of phase change from -180^o to +180^o, it is felt that by using the final improved model this performance could be predicted well. The magnitude of phase change is large, at 15GHz a continuously variable phase shift between 0^o and 90^o is obtained at through transmissions better than -13dB.

In order to investigate the resonance effect a passive line Schiffman section was fabricated and measured. Two 50Ω coupled lines, width=0.59mm, ϵ_r=10.5, height=0.635mm, spacing=0.4mm, were shorted at one end of the coupled region, length=6.5mm and results are shown below

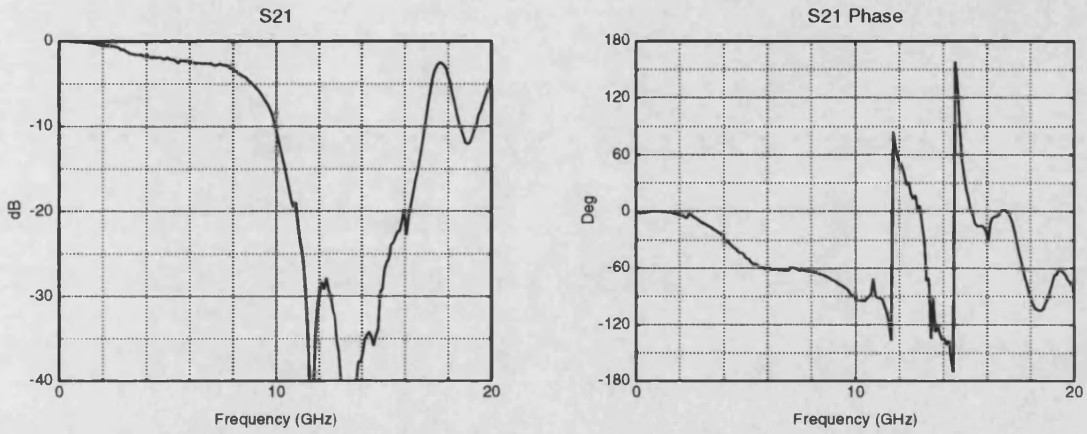

Figure 6.4: Measured results for passive microstrip Schiffman phase shifter

These results show clearly the non-linear phase shift in the low frequency region used to obtain the fixed differential phase shift. At higher frequency resonant behaviour is observed, similar to that found in the wide FET.

FET 2 was then configured as phase shifter and the measured results are shown below

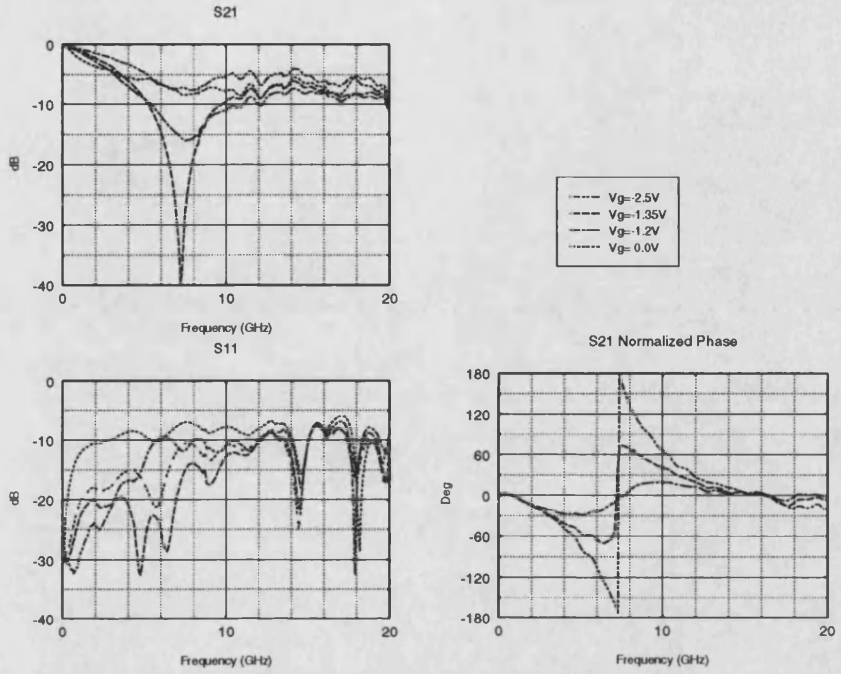

Figure 6.5: Measured results for FET 2 Schiffman phase shifter

Again good variable phase shift performance is observed either side of the resonance. At 4GHz a phase shift of 60° is obtained with through transmission better than -7dB and at 10GHz 60° phase shift occurs with through transmission better than -12dB. The resonance is observed to be much lower in frequency than for FET 1 supporting the fact that it is related to coupled region length.

FET 3 was then measured as a phase shifter the results are shown in figure 6.6

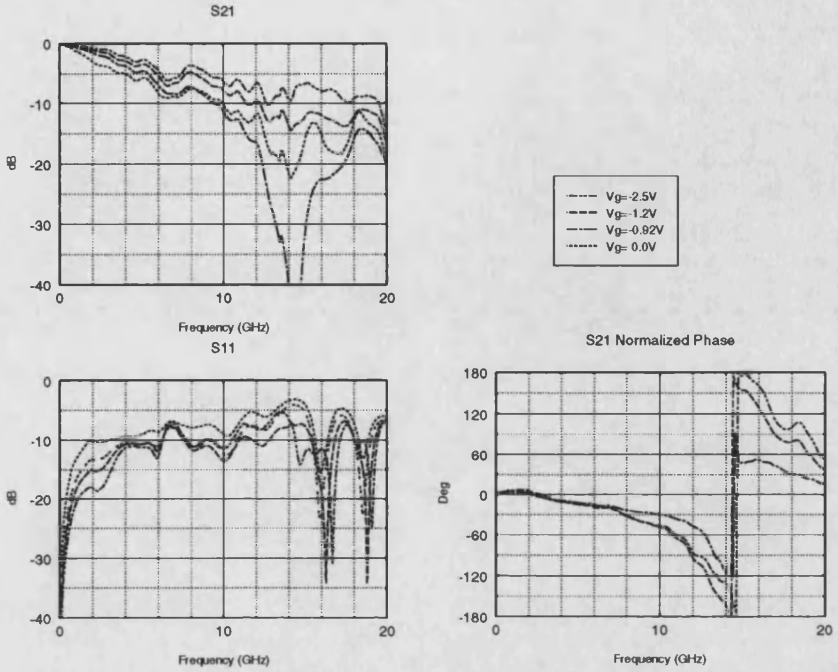

Figure 6.6: Measured results for FET 3 Schiffman phase shifter

As expected the resonance has shifted up in frequency to 14GHz. The phase shifter performance is slightly less good than that for FETs 1 and 2 with 50° phase shift at 10 GHz.

To investigate the performance of the wide FET as a differential phase shifter the adjustable electrical delay facility available on the HP8510B VNA was used. In a differential phase shifter half of the incident power would be passed through a linear phase shift and half through the wide FET, the difference between the phase of the two signal paths being fixed over a band of frequencies. To simulate this, linear phase shift equivalent to that in an ideal 50Ω transmission line is added to the phase response of the wide FET. The total phase response is then equivalent to the difference between the wide FET phase response and that of a 50Ω transmission line of a certain length. The results for FET 2 are shown below

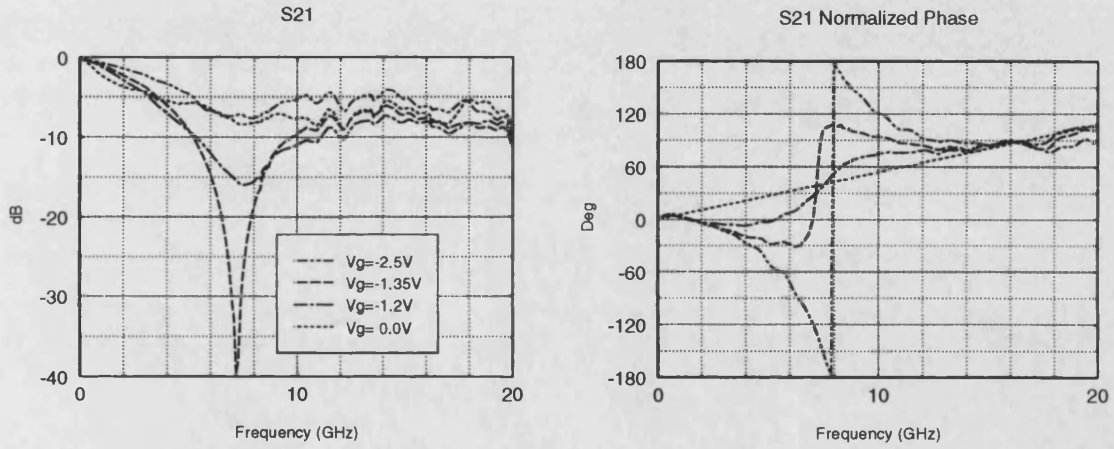

Figure 6.7: Measured results for FET 2 Schiffman phase shifter relative to length of transmission line

The zero bias phase response shows the linear phase added to the wide FET response. It is seen that a relatively constant phase shift is obtained in the high frequency region at reasonable through transmission levels.

6.2.4 Conclusions

A wide FET has been configured as a two-port phase shifter and modelled and measured results have been shown. The model predicted large phase shifts at reasonable through transmission levels and measured results showed this to be the case. Three different wide FETs were measured and showed similar performance, a resonance in the magnitude of the through transmission appears to be related to the coupled length of the structure. This resonant behaviour is also observed in passive lines. Finally the wide FET was measured in a simulated differential phase shifter mode and showed wideband, reasonably constant phase shift performance. This section has shown the potential for use of wide FETs in phase shifting applications.

6.3 Tandem Connection of Two Wide FETs

6.3.1 Introduction

It is well known that two directional couplers can be connected together in such a way as to produce a directional coupler with higher backward coupling [107]. Using this technique very high backward coupling levels can be obtained $\simeq$-3dB, remembering that the wide FET directional coupler had low through transmission, then if the backward coupled port is configured as the through transmitted port, improved coupler performance could be possible.

6.3.2 Modelled Results

This application was initially investigated using the wide FET model at a stage where gate masking and extra C_{ds} had not been added. The modelled results for two FET 1 devices connected in tandem with open circuit gate lines are shown below

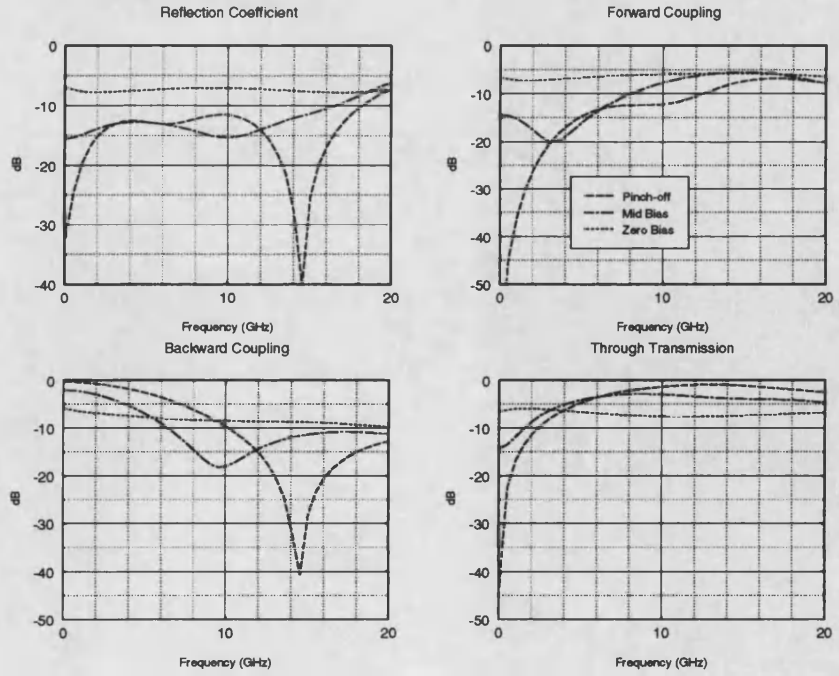

Figure 6.8: Modelled results for FET 1 tandem coupler

The through transmission is seen to be very high around 12GHz, however, the coupler is in fact a forward, rather than backward coupler at these frequencies. At 8GHz the through transmission is reasonable and at pinch-off backward coupling is observed but with low directivity.

6.3.3 Measured Results

The modelled results suggested that this method could increase the through transmission to more realistic levels, thus two FETs were connected in tandem with open circuit gates, the devices were configured as shown below

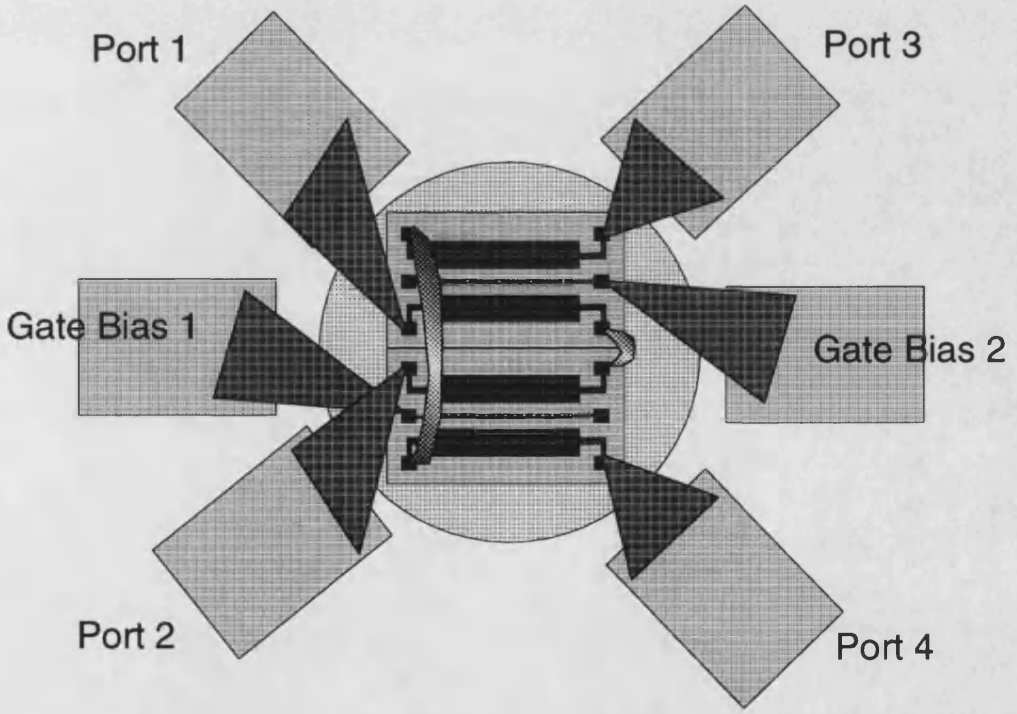

Figure 6.9: Measured results for FET 1 tandem coupler

The figure shows that the tandem connection is not straightforward and requires long tape bonds. This configuration was measured, the results are shown in figure 6.10

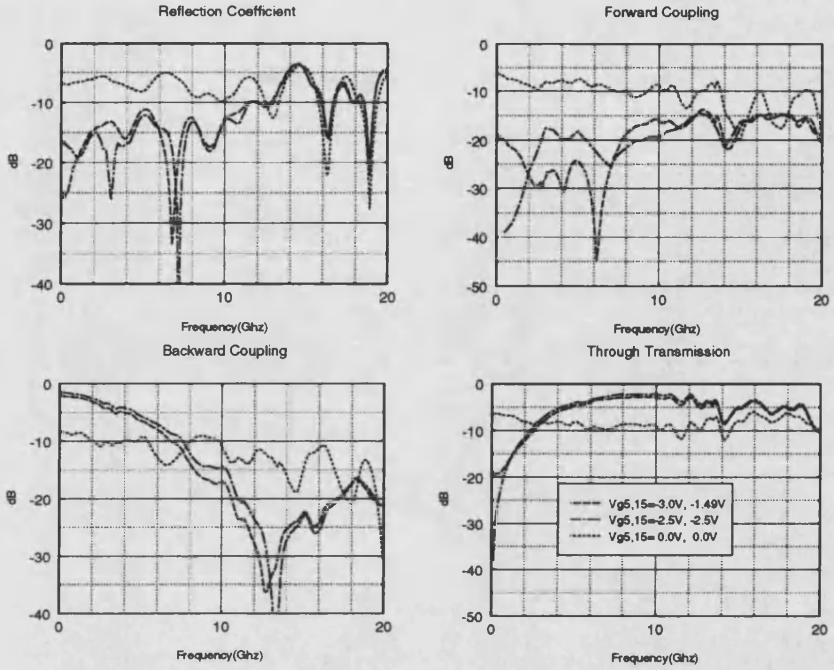

Figure 6.10: Measured results for FET 1 tandem coupler

The general trends observed agree with those of the model. The through transmission is high around 10GHz, however, the coupler does not exhibit substantial directivity. Around 6GHz reasonable coupler performance is obtained, however, the coupler does not have the same amount of tunability as observed in the single FET results.

These results, while not being an improvement on the single FET results, were encouraging, in that the level of the through transmission could be increased. Thus it was felt that by integrating the two FETs together, on-chip, the reduction in parasitic inductances could improve the performance.

An integrated design was therefore produced, the basic device was the FET 3 device, the initial FET 3 device had not been fabricated at this point and its poorer performance had not been measured. The layout for the integrated tandem coupler is shown below

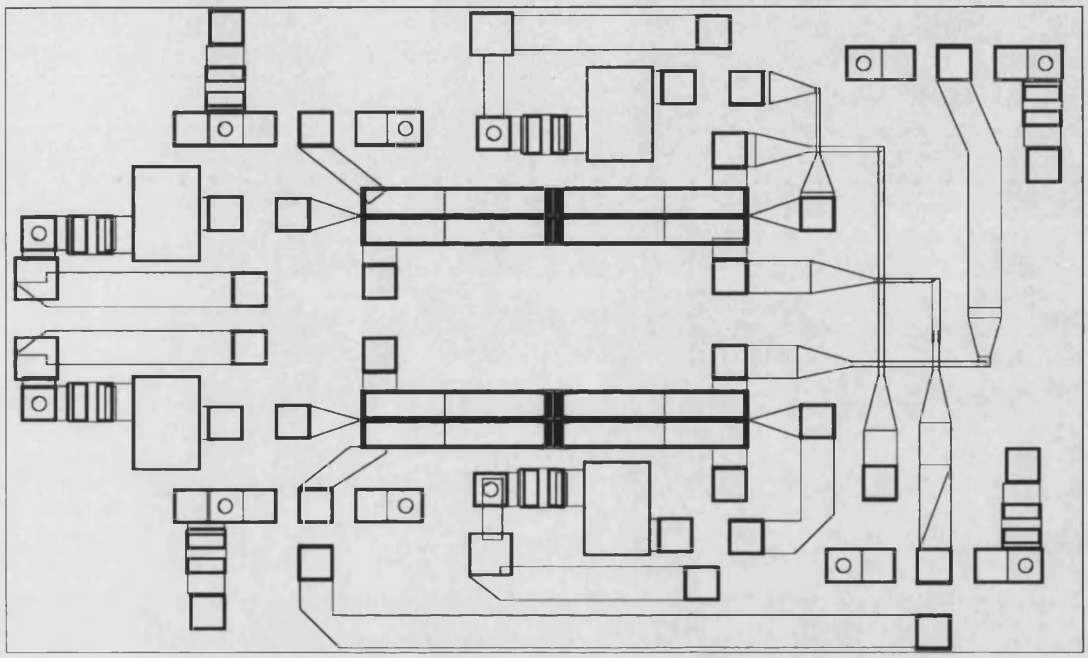

Figure 6.11: Integrated tandem coupler

The chip measures 3.8mm x 2.3mm. The layout is complicated by the fact the the tandem design was made compatible with Schiffman phase shifter design, hence the long transmission line which would be used for shorting two ports of the coupler. The chip also contains optional gate terminations and optional port terminations. All the functions on this chip have not been characterized and could be the subject of future work. The measured results are shown overleaf.

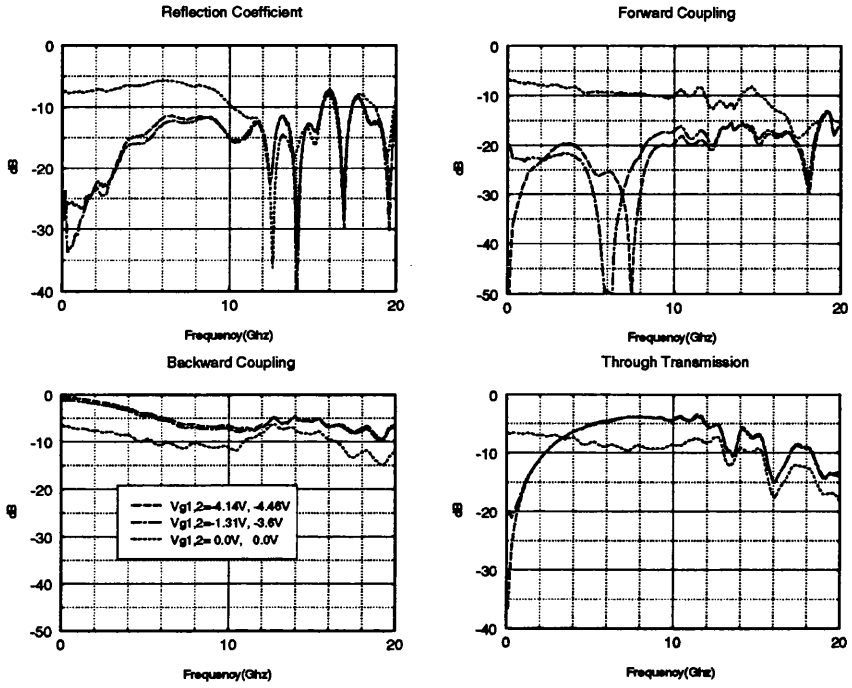

Figure 6.12: Measured results for integrated FET 3 tandem coupler

The results show similar trends to the non-integrated version but with much reduced forward coupling. The through transmission is reasonable from 5GHz to 12GHz with better than -5dB and across this band the backward coupling varies from -4dB to -7dB. The forward coupling has a large resonance which is tunable in the 6GHz to 8GHz range. The through transmission could be improved by using FET 1 as the basic element since this has higher backward coupling, this would result in higher through transmission for the tandem design. For comparison with the single FET results the directivity and backward coupling are plotted across the optimum performance bandwidth, shown in figure 6.13

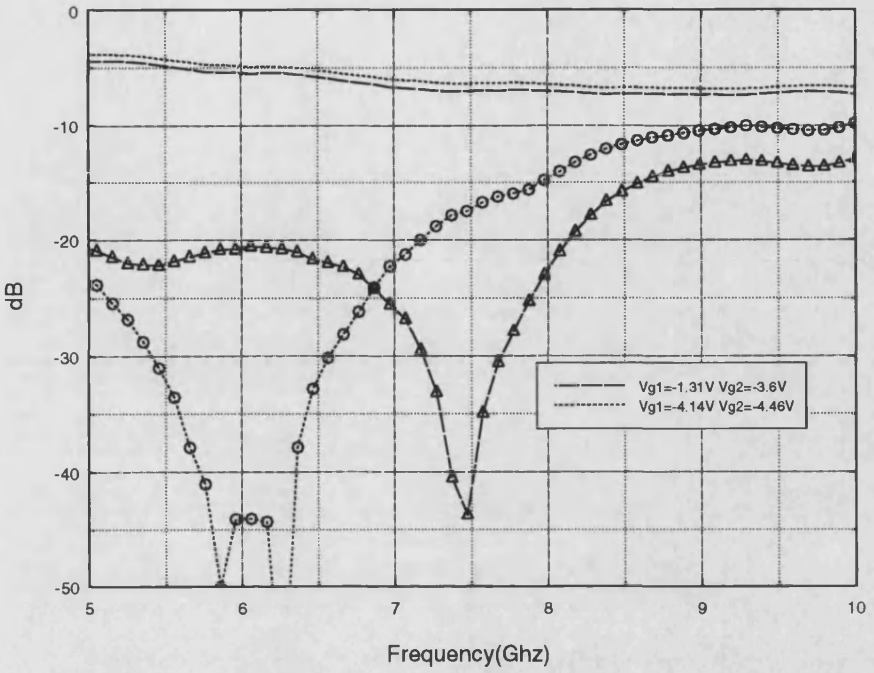

Figure 6.13: Measured results for integrated FET 3 showing directivity (marks) and backward coupling (lines)

The results show the very high directivities obtained from this design. These measurements were performed with open circuit gate lines, the use of 50Ω terminated gate lines could further improve this performance. This device could therefore be used to perform accurate return loss measurements on-chip. The tunability of the device extends the band over which these measurements could be made to ≃2GHz. The through transmission and reflection coefficient are shown in figure 6.14

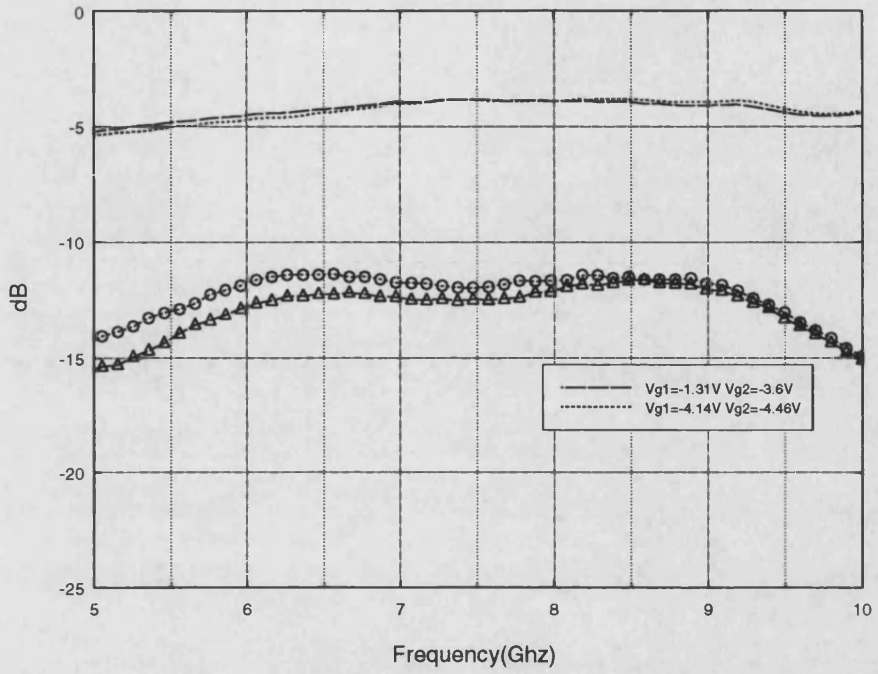

Figure 6.14: Measured results for integrated FET 3 showing reflection coefficient (marks) and through transmission (lines)

The through transmission is reasonable but still less than that achievable with a purely passive design, however, by using basic FETs with higher coupling this could be improved. The reflection coefficient is also found to be reasonable, better than -11dB across the band.

6.3.4 Conclusions

It has been shown how two wide FETs can be connected in tandem to produce a directional coupler with reasonable through transmission and high, tunable directivities. By using FETs with higher backward coupling this performance could be improved upon.

6.4 Summary

In this chapter two examples of applications of tunable coupled line structures have been investigated. In both cases, initial investigation was carried out using the model that has been developed in this work. The multiport connection method [79] was used to connect the basic wide FET model into the new configurations, thus no commercial simulator was required.

The first application was that of a Schiffman phase shifter. All three wide FET structures were configured as phase shifters and for FET 2 continuously variable phase shift from 0^o to 90^o at 15GHz was obtained. When used as a differential phase shifter relatively constant phase shift across a wide band was obtained.

Secondly two wide FETs were connected in tandem [107] to produce high backward coupling which could be used as a through path. Using two wide FETs high backward coupling was obtained, however, the coupler performance across this band was not good. An integrated design was fabricated with two wide FETs and reasonable through transmission was obtained with very high, tunable directivities.

These applications show the potential of wide FETs used as tunable coupled line structures. Wherever passive coupled lines are used, the wide FET could be used to introduce flexibility and on-chip tunability. A number of other applications will be discussed in the final chapter.

Chapter 7

A Planar Schottky Barrier Diode

7.1 Introduction

Schottky barrier diodes are formed when a metal is brought into contact with a semiconductor with an appropriate work function [110]. These type of contacts were were first implemented more than one hundred years ago using the whisker diode configuration [110] where a very fine wire of metal is brought into contact with a semiconductor. This type of diode, whilst very popular, was very unreliable and it was not until the 1950s [110] when thin films could be evaporated onto semiconductor surfaces that reliable diodes could be formed. P-N junction diodes became available around this time but due to the fact that minority carriers take a finite time to diffuse when the diode is switched they have much higher capacitance than the Schottky diode which is a majority carrier device [104]. Thus at microwave frequencies where low capacitance is of the utmost importance the Schottky barrier diode became the standard diode.

Schottky barrier diodes have many applications, including mixer diodes and detector diodes, at present they are widely available as discrete devices on GaAs but are not yet readily available in MMIC form from all foundries [24]. If diodes are required they are usually formed from standard FET structures by shorting drain to source [111]. These diodes,

however, are large structures, typically for a 4x75μm FET the area is 22500μm^2, neglecting bond pads. These diodes are sufficient for varactor applications, where large capacitance variations are required, however, for low capacitance applications their performance would be poor.

This chapter discusses two Schottky barrier diodes manufactured using a standard foundry process, through the GMMT foundry, towcester, UK. The diodes have a very simple construction resulting in much reduced device areas. The first diode has a junction width of 115μm, this was chosen to give capacitances large enough for varactor diode applications to be discussed later. A schematic of the device is shown in figure 7.1

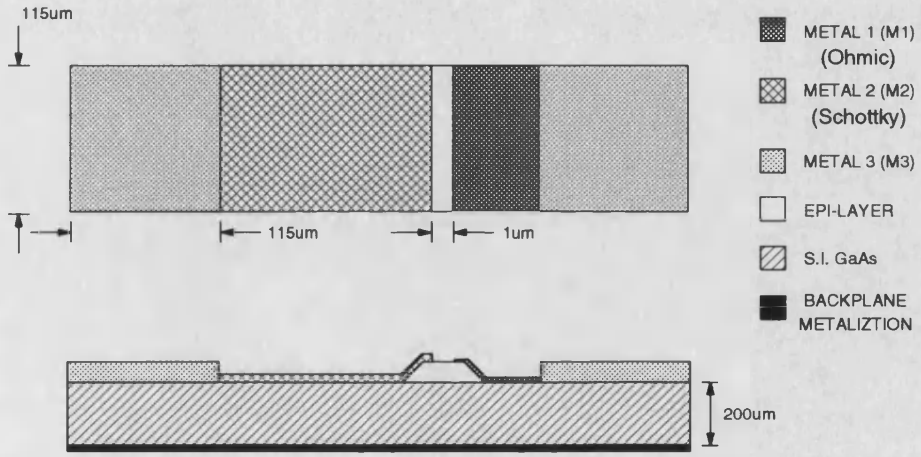

Figure 7.1: A monolithic Schottky barrier diode

The diode is formed by overlapping a small area of metal 2 (M2) onto the ion-implanted n-mesa to form a Schottky contact, an ohmic contact is formed on the opposite edge of the mesa using M1. These contacts are then connected to M3 bond pads. The second diode is similar in construction to that in figure 7.1, however, the junction width is reduced to 19μm, giving a much smaller depletion capacitance, resulting in improved performance in such applications as microwave detection. These diodes result in a reduction in device area of 56:1 and 45:1 for the narrow and wide devices respectively when compared with a 4x75μm FET used as a diode.

In this chapter these diodes are characterized at both d.c. and microwave frequencies. The standard diode model has been used to model the devices and good agreement between measured and modelled results has been obtained. The diodes are then configured as microwave detectors and their performance is compared up to 20GHz. Finally, the diodes are used as varactors in a phase shifter application and good performance is obtained.

7.2 D.C. Characterization

The GaAs chips were mounted in microstrip test fixtures similar to those used in chapter 4, but consisting of only two microstrip lines on 0.635mm thick, ϵ_r=10.5 RT-Duroid^{TM}. The d.c. I-V characteristics were measured and using a technique outlined in [112] and discussed below, where log(I) is plotted against voltage a number of important diode parameters can be calculated. The log(I) vs V plots are shown below

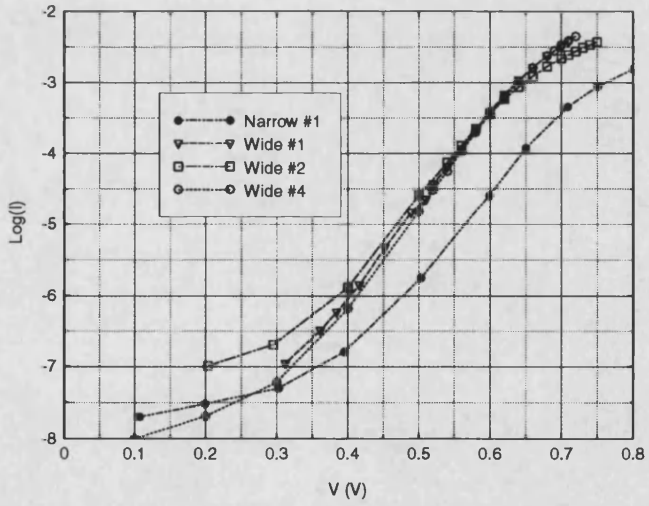

Figure 7.2: Log current vs voltage for wide and narrow Schottky diodes

The figure shows results for three wide diodes and one narrow diode. All the devices show the same form : a central linear section and non-linear regions at high and low current levels. It can be shown [112] that the intercept of the gradient of the central section with the current axis gives the log of the reverse saturation current. From this the barrier height from metal to semiconductor can be calculated. The central section is the diodes square-law region and

is therefore linear when plotted logarithmically. From the change in voltage over one decade of current the ideality factor of the diode can be determined. At high current levels the junction resistance of the diode becomes very small and the series resistance of the diode starts to dominate, thus plotted logarithmically this will be non-linear. The series resistance is calculated from the magnitude of the deviation from linear at a particular current level. It is noted in figure 7.2 that the narrow diode will have a very different intercept on the current axis, this is because the area of the diode is much smaller and therefore the magnitude of the reverse saturation current will be smaller. In calculating the barrier height, it is current density rather than current which is used and thus similar results will be obtained as will be shown below. The parameters discussed above have been calculated for the four diodes and are shown in table 7.1

Device Type	Wide			Narrow
Device Number	1	2	4	1
Series Resistance, $r_s(\Omega)$	11.1	17.4	9.2	33.4
Barrier Height, Φ_b(V)	.386	.421	.377	.438
Ideality Factor, n	1.383	1.47	1.29	1.55

Table 7.1: D.C. parameters of wide and narrow Schottky barrier diodes

The figures for Φ_b are somewhat different from the barrier heights quoted in the literature, Sze [104] quotes $\Phi_{bAu-GaAs}$=0.9V. However, Rhoderick [110] states that the phenomenon of surface states, which exist at the surface of a semiconductor due to incomplete inter-atomic bonds, can have the effect of reducing the barrier height and can also make the barrier height independent of metal work function. At the time of writing no data on barrier height was available from GMMT and it may be that surface states are causing this reduction in barrier height. The ideality factors are much higher than the 1.04 given in [104], however these figures are for vertical, not planar devices. In [113] an ideality factor of 1.5 was reported for a planar structure. The series resistance agrees well with those values reported in the literature and the narrow diode has a higher series resistance as might be expected. However, the ratio of series resistance for the two devices should, in the ideal case, be in ratio of their junction widths, however, this is not the case. The repeatability of the d.c. parameters

is seen to be low, especially for the series resistance, this is most likely caused by process variation and might explain the discrepancy in the series resistances. More devices need to be measured to obtain a better estimate of all the d.c. parameters. Thus the four devices have been characterized at d.c. and the important d.c. parameters have been calculated.

7.3 Microwave Characterization

The diodes were mounted in microwave test fixtures described above and the S-parameters were measured at various bias levels. A simple model for the diode was fitted to this data to determine the level of junction capacitance of the diodes. The model consisted of a parallel R-C representing the diode junction resistance and capacitance, a series resistance and input and output connection inductances. The results are shown in figure 7.3 for the wide diode

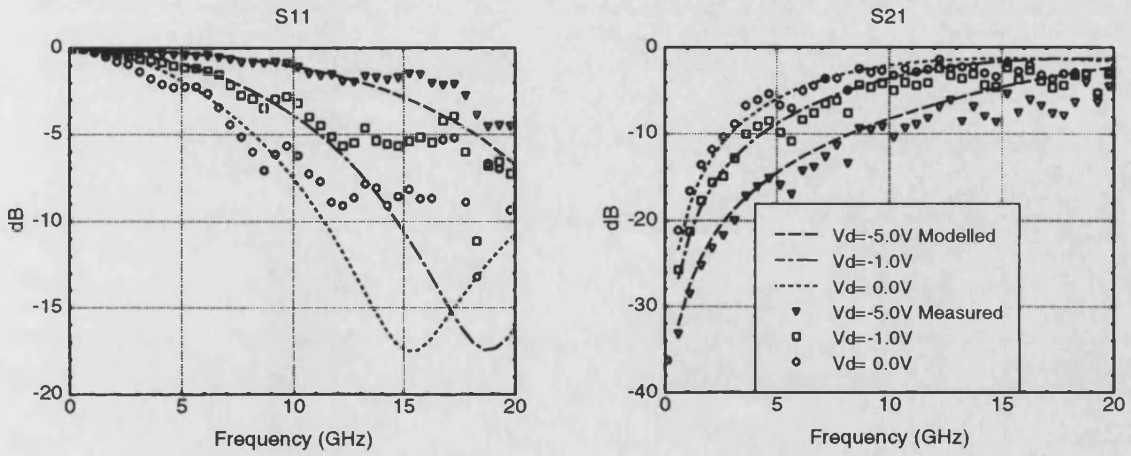

Figure 7.3: Measured and modelled S-parameters for wide Schottky barrier diode

The model values used were : series resistance, 15Ω, connection inductance, 0.3nH, junction resistance, 10KΩ and junction capacitances of 0.18pF, 0.12pF and 0.06pF at 0.0V, -1.0V and -5.0V, respectively. The results show that the diode is reasonably well modelled by this simple model. Ideally the diode should appear as an open circuit, however, the large junction capacitance is shorting out the junction at higher frequencies increasing the through transmission and decreasing the reflection coefficient.

The narrow diode was measured and modelled, the results are shown in figure 7.4

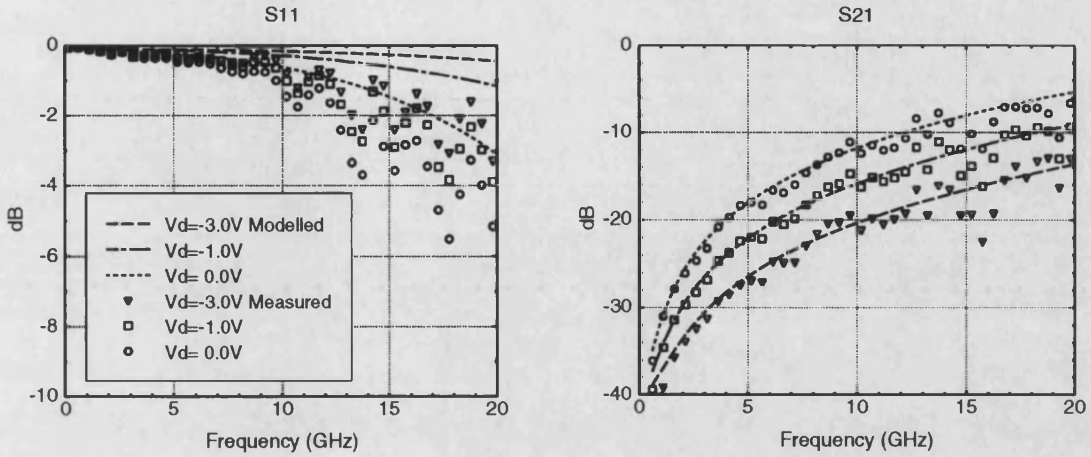

Figure 7.4: Measured and modelled S-parameters for narrow Schottky barrier diode

The model values used were : series resistance, 33Ω, connection inductance, 0.3nH, junction resistance, 10KΩ and junction capacitances of 0.04pF, 0.025pF and 0.015pF at 0.0V, -1.0V and -3.0V, respectively. Again reasonable agreement is shown. The level of the through transmission is much lower reflecting the much lower junction capacitance of the narrow diode.

Thus two Schottky barrier diodes have been measured and modelled from 0.1GHz to 20GHz and good estimates of junction capacitance have been made. The narrow diode has been found to have very low levels of junction capacitance, making this diode useful in such applications as microwave detectors, this application will be discussed in the next section.

7.4 Schottky Barrier Microwave Detectors

Schottky barrier diodes have been used as detectors since the beginning of this century [110]. Once a rectifying contact is formed the principle behind detection is straightforward. If a time varying signal is incident upon the diode, the transmitted signal is rectified and thus possesses a d.c. level. If the diode is operated in its square-law region the d.c. diode current is proportional to the incident power. This is a very useful feature of diode detectors, but normally limits their use to low power applications, where the diode can operate in square-law.

The two diodes were configured as detectors and their sensitivities, in millivolts of d.c voltage per milliwatt of microwave power, were measured from 0.1GHz to 20GHz at two different power levels, -5dBm and -15dBm. The input power levels were measured at each frequency into a matched load. The diodes were forward biased to 80μA, this gave the optimum sensitivity.

The results for wide and narrow devices are shown in figures 7.5a and 7.5b respectively

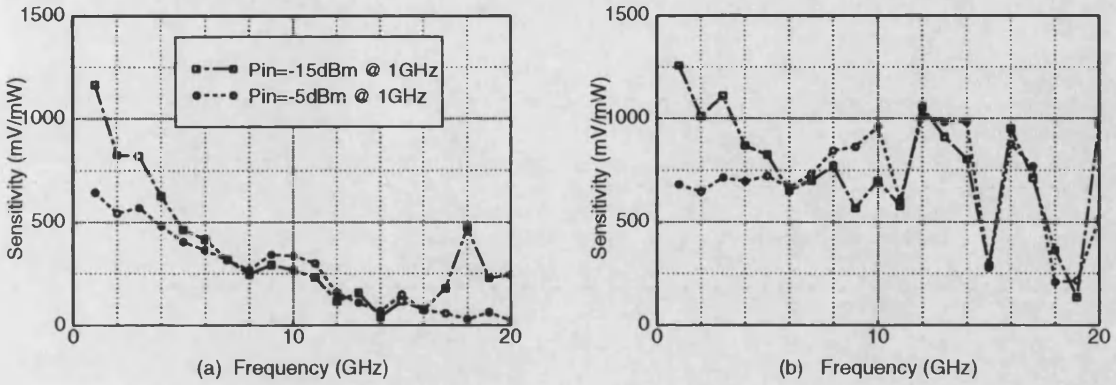

Figure 7.5: Microwave sensitivity : (a) Wide diode (b) Narrow diode

At low frequency $\simeq$1GHz both diodes have similar sensitivities, as the frequency increases, the wide diode sensitivity drops dramatically due to the large junction capacitance. It is seen at low frequency that the diodes are more sensitive to low powers, where the diodes are in their square-law region. The narrow diode exhibits good sensitivity across a very broadband, the average sensitivity is $\simeq$600mV/mW, this compares well with manufacturers data, for example Hewlett Packard quote 400mV/mW for a matched 0.01GHz - 12GHz detector [114]. The detector in this work is unmatched, however, the sensitivity is such that broadband matching, such as 50Ω in parallel with the diode could be used and reasonable sensitivity maintained.

Thus two Schottky barrier diodes with different junction widths have been configured as detectors and their characteristics measured. The narrow diode exhibits good sensitivity across a broadband from 0.1GHz to 18GHz. This shows one of the many applications for low junction capacitance diodes that cannot be implemented on MMIC by using standard foundry components such as an FET with source and drain shorted together. In the next section these monolithic diodes will be configured as varactors and shown to have good performance.

7.5 Varactor Diode Controlled Phase Shifters

Varactor diodes are widely used in phase shifting applications [111, 115]. Continuously variable phase shifters are required in many applications especially phased array radar systems where the phase shift of many feed lines needs to be controlled accurately [9]. Continuously variable diode phase shifters are generally of two types (i) reflection [111], (ii) loaded-line [115].

A reflection-type phase shifter generally uses a 3dB hybrid coupler and two varactor diodes connected to the backward coupled and transmitted ports of the coupler. Assuming an ideal coupler and lossless diodes, power incident on the coupler will split equally between the two varactors and will be reflected back to both the input and the output of the coupler. This will produce two signal components at both input and output and because of the phase shifts introduced by the coupler the signals at the input will cancel and those at the output will add in-phase. Thus all power incident on the coupler will pass to the output with a phase shift determined by the reactance of the varactors. These type of phase shifters give very broadband performance, but require the design of a broadband hybrid 3dB coupler.

In this section a loaded-line phase shifter is designed using the Schottky diodes characterized in the previous sections. This type of phase shifter is simpler to implement, but gives narrower band performance compared to the reflection-type. The loaded-line phase shifter uses the fact that a small reactance placed in parallel with a transmission line will produce a phase shift in the transmitted signal dependent upon the level of the reactance. Thus if the level of the reactance can be tuned electronically, a variable phase shifter can be implemented. If a single reactive element is used the reflected signal can limit the performance of the phase shifter [9]. However, if two reactive elements are placed one quarter wavelength apart then the reflected signals will destructively interfere at the input producing a well matched device. This will only be true for a narrow band of frequencies, however, as will be shown here, reasonable performance is obtainable using this technique.

A loaded-line variable phase shifter was implemented using the GMMT F20 process. A length of 50Ω transmission line was defined with three different diodes placed at either end of the line, allowing for each to be bonded in place to evaluate their performance separately. The layout for the circuit is shown below

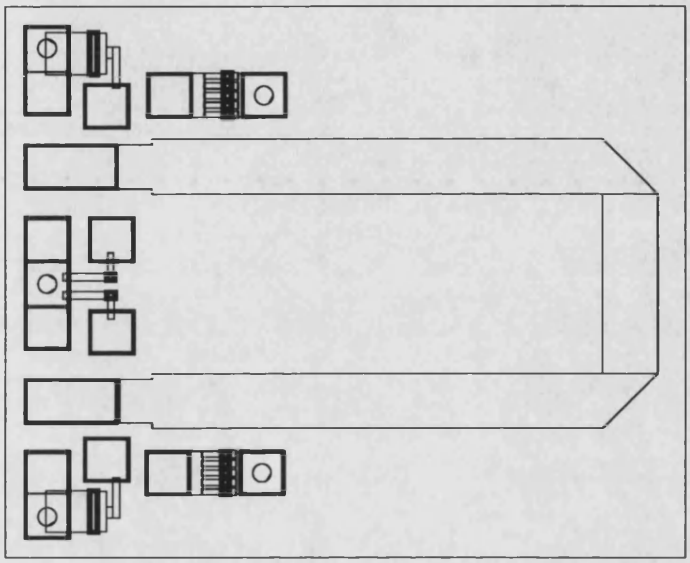

Figure 7.6: MMIC loaded-line phase shifter

The chip dimensions are 2.7mm x 1.6mm. The line length between diode connection pads is 330μm, this has a quarter wavelength frequency of 8GHz thus well matched performance should be obtained around this frequency. There are three different diodes available on-chip, a standard wide diode, a narrow diode, and a wide diode formed from five narrow diodes connected in parallel. It was felt that the combination of five narrow diodes may give lower series resistance than the wide diode since from d.c. measurements the wide diode had only half the series resistance of the narrow diode but was approximately fives times as wide.

The MMIC chips were mounted in microwave test fixtures and measured from 0.1GHz to 12GHz. The results are shown in figure 7.7 for the five narrow diode combination

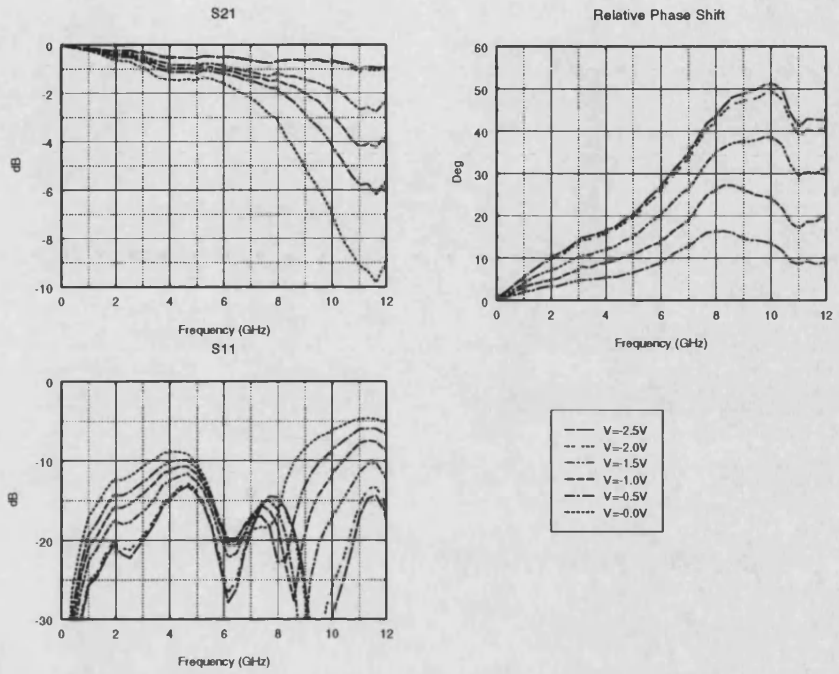

Figure 7.7: Measured results for MMIC loaded-line phase shifter

The results show through transmission, S_{21}, reflection coefficient, S_{11}, through phase shift normalized to the zero bias sate. It is seen in the zero bias state the through transmission is at its lowest since the junction capacitance is at its highest value. As the negative bias increases, the through transmission increases as the junction capacitance decreases. The relative phase shift is seen to become more positive as the negative phase shift of the capacitance is removed. The phase shift is seen to be approximately proportional to frequency over much of the band, this implies a constant time delay for the circuit. It is well known that this feature is required for broadband phased array operation [116], [117] . The reflection coefficient is reasonable around the design frequency of 8GHz, being better than -14dB and the through transmission is better than -3.1dB for all bias states. The through transmission levels are similar to those reported by Lucyszyn [111] where standard foundry FETs were employed as varactors in a reflection-type phase shifter and by Wilson *et al* [116].

The linearity of phase shift against the tuning voltage was also investigated and is shown below

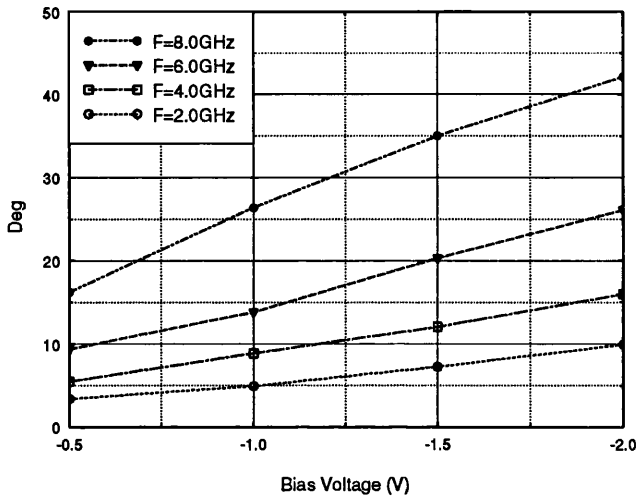

Figure 7.8: Phase shift linearity with tuning voltage

It is seen that from 0.5V to 2.0V approximately linear tuning is obtained, this would be advantageous in many applications.

Thus a loaded-line phase shifter has been implemented in monolithic form using standard foundry processing. Continuously variable phase shifts of 0^o to 43^o at 8GHz and 0^o to 26^o at 6GHz have been obtained at through transmission levels better than -3.1dB and -1.6dB respectively. The phase shifter exhibits phase shift proportional to frequency, or constant time delay, which is advantageous in phased array applications. The diodes employed have very simple construction and occupy minimal substrate area. The diode active layer has not been optimized for varactor operation, if this was available, lower series resistance and greater capacitance variation could be obtained. The performance of the other diodes fabricated on-chip could be the subject of future work.

7.6 Summary

In this chapter two monolithic planar Schottky barrier diodes have been fully characterized at d.c. and microwave frequencies from 0.1GHz to 20GHz. The diodes have a very simple construction and the device areas are in the order of fifty times smaller than diodes implemented using shorted FETs. The two diodes have different junction widths, one of 115μm for varactor applications and one of 19μm for detector applications. The diodes have been configured as detectors and good broadband performance obtained with average sensitivities of 600mV/mW from 0.1GHz to 18GHz. Five narrow diodes, connected in parallel, were then integrated into a monolithic loaded-line phase shifter circuit and good performance was obtained. Continuous phase shift from 0° to 43° at 8GHz was obtained, and constant time delay performance was obtained up to 8GHz, making the phase shifter useful in phased array applications.

This chapter has shown that high performance Schottky barrier diodes can be implemented using standard foundry processes. They have advantages of smaller size and simpler construction when compared to shorted FET diodes. If the active layer characteristics were optimized for different applications further improvements in performance could be obtained.

Chapter 8

Conclusions and Further Work

8.1 Summary of Thesis

The aim of this work was to design novel monolithic microwave devices, within the limitations of standard foundry processes. The majority of this work deals with the wide FET structure, where a FET is made wide enough such that distributed coupling effects are observed between the electrodes. The wide FET has been shown in a new type of configuration, as a six-port, where the source, gate and drain lines are considered as coupled microstrip lines. It has been found that the forward coupling between source and drain lines can be controlled by the d.c. gate bias. When the channel resistance is high (>100Ω), the backward coupling remains relatively constant with gate bias and the forward coupling is tunable, giving rise to voltage controlled directivity.

In chapter 2 a model for the wide FET is developed, it is believed by the author that this is the first such analysis of a wide FET in the switching configuration, where there is no d.c. source - drain current and the source line is ungrounded. The model has been used extensively in this work to predict the performance of wide FET structures. In particular the model highlighted the increased directivity obtainable with 50Ω terminations added to the gate line. The introduction of the effect of the gate depletion region on the inter-electrode

capacitances, termed "gate masking" and extra drain - source capacitance associated with the proximity of the drain and source ohmic contact regions, improved the fit of the model to measured data. The final model simulates the performance of the three wide FET test structures well.

In chapter 3 issues associated with measuring multiport active devices are discussed. The test fixture used in all subsequent microwave measurements is described in detail, showing how repeatable, low parasitic connections are made to the monolithic devices. When measuring devices with more than two ports on a two-port network analyser, the idle ports are terminated in 50Ω. Expressions are derived that are used to estimate the effect of the idle terminations on the transmission parameters of multiport devices. The use of on-wafer probing to measure the performance of multiport MMICs, unaffected by connection parasitics is then discussed. In order to apply d.c. bias to active devices, broadband bias circuits are required that do not affect the microwave performance of the device. The design of these is discussed, in particular broadband choke coils. Finally, an estimate of the parasitics associated with the microwave test fixtures is obtained for use with the model developed in chapter 2.

In chapter 4 a wide FET is configured as voltage controlled directional couplers and is fully characterized from from d.c. to 20GHz. The initial test fixture used to measure the first FET structure was seen to dominate the device performance, with reduced parasitics, improved directional coupler performance is obtained. The model developed in chapter 2 is used to investigate the effect of different gate terminations, and it is found that improved directivity is obtained with 50Ω added to the gate line. This is implemented and found to be the case. Terminating the gate line in 50Ω leads to full six-port characterization of the device, which in turn leads to the inclusion of gate line resistance in the model. The model is then fitted to measured data for FET 1 and a reasonably good fit obtained.

In chapter 5 the second wide FET test structure, with different electrode geometry is characterized and good voltage controlled directional coupler performance obtained. The model

is fitted to the measured data, the fit is however, less good than for FET 1. The third FET structure, the geometry of which was predicted by the basic model as having high directivity, is measured and found to have poor performance. This results in further model improvements, with the inclusion of gate masking and extra drain - source capacitance. The final model is then fitted to the measured data for all three devices and a good fit is obtained. Finally the model is used to predict the performance of the devices with much reduced parasitic inductance, very good performance is predicted, with greater than 20dB directivity from 5.5GHz to 10.9GHz at a nominal coupling of -7.9dB and a coupling flatness of $\pm$1.75dB. Moreover this directivity is tunable and the frequency of maximum directivity can be tuned from 5.0GHz to 9.0GHz.

Thus a novel voltage controlled directional coupler is presented that combines passive microwave techniques with the Schottky barrier contact layer available to the MMIC designer to obtain a voltage controlled device that has tunable directivity. This device could have many applications, including in microwave measurement systems where high directivity is very desirable. The tunability could increase yields for devices with tight specifications and if integrated into a monolithic multifunction circuit, the tunability would allow post-fabrication "tweaking" of system performance - a luxury not often available to the MMIC designer.

This tunable coupler could have many other applications, some of which are discussed in the further work section. As examples of these, in chapter 6, the wide FET is configured as a Schiffman phase shifter, where source and drain lines are shorted together at one end to form a coupled, meandered section. Continuously variable phase shift from 0^o to 90^o is obtained at 15GHz. When configured as a simulated differential phase shifter, wideband constant phase shift is obtained.

The second application is as a tandem coupler, where two wide FETs are connected such that the backward coupling is very high and can be used as the through transmission path. Reasonable performance was found with two discrete wide FETs tape bonded together, and a fully integrated design was carried out which produced reasonable through transmission

and very high tunable directivity.

Finally chapter 7 investigates another monolithic device, a planar Schottky barrier diode. The device is often implemented using an FET with source and drain shorted together and is not widely supported as a foundry standard library element. This chapter shows an easy to fabricate diode with a very small device area, in the region of fifty times smaller than a shorted FET design. Two devices are fabricated, a narrow device for detector applications and a wide device for varactor applications. Both devices are characterized at d.c. and microwave frequencies and are configured as detectors, the narrow diode shows good performance, comparable with commercially available devices. Five narrow diodes connected in parallel are then integrated into a loaded-line phase shifter and good, continuously variable, constant time delay performance is shown, which is ideally suited to phased array applications.

Thus, two novel monolithic devices have been presented, fabricated using standard foundry techniques. The concept of the Schottky barrier microstrip line has been extended to three coupled lines and tunable directivity couplers have resulted. A simple, reduced size Schottky diode has been shown to perform well in two different applications. This work highlights the potential for innovation that the monolithic process offers the microwave designer. In the coming years it is felt that foundries will allow more "custom" designs to be undertaken which stray from their standard library of components. Eventually designers may have control over fundamental process parameters such as gate length, implantation depth and doping profile. This will open up still further horizons for creating completely new devices.

8.2 Further Work

There are a number of areas in which this work could be extended, these are grouped into three areas : modelling, measurements and applications.

8.2.1 Modelling

Having obtained a good model for the wide FET, the propagation characteristics of the structure could be investigated. The propagation constants, mode impedances and mode voltage solutions of the structure could be used to investigated the resonance phenomenon observed in the forward coupling between source and drain lines.

The physical basis of the wide FET model could be enhanced whereby the FET model parameters are related directly to the geometry and doping of the FET structure. Further improvements would be to relate the model parameters directly to the applied gate voltage, allowing S-parameters at a given voltage to be calculated.

The calculation of inter-electrode capacitance could be improved by introducing graded mesh techniques around the gate line. The effect of source and drain line thickness could also be further investigated. Other methods of calculation could be used that take into account effects like dispersion and skin effect, allowing the model to be used at higher frequencies.

The model of the test fixture could be improved by including the microstrip connection lines and connector transitions. The effect of d.c. blocking capacitors and choke coils could also be included. With the inclusion of the microstrip connecting lines, the phase response of the S-parameters could be investigated as a further aid to fitting the modelled to measured data.

8.2.2 Measurements

The major requirement is to carry out on-wafer measurements of the wide FET devices, initially, simply with a two-port network analyser, then using switching networks such that all ports of the device can be ideally terminated. This would allow the intrinsic performance of the device to be measured.

The use of on-chip terminations could be investigated. Once a high performance on-chip 50Ω load had been designed, the idle ports of the device could be terminated, giving close to the intrinsic performance of the device.

Narrower FETs could be fabricated which should have tunable performance at higher frequencies, provided the FET capacitances are not too high. The model could be used to investigate this high frequency region, bearing in mind this is only a quasi-TEM model. Other device types such as HEMTs could be investigated for use in this high frequency region.

Meandered FETs could be fabricated that reduce the device area, making these devices more cost effective. Models for these devices could also be developed.

Three or more FETs could be meandered and connected in parallel with a Chebychev or maximally flat coupling profile to further improve the directivity of these devices. Each section could be independently tunable to obtain maximum performance.

8.2.3 Applications

Other applications for the wide FET structure could be as a variable Wilkinson divider, where the source and drain lines are shorted at one end to form a three-port device similar to a Wilkinson divider. The tunability provided by the wide FET could produce a useful new type of device.

Further tandem coupler designs with higher backward coupling for the individual FETs would produce higher through transmission.

Other configurations for the wide FET could use the non-linearity of the FET model elements to perform mixing operations. The multiport nature of the device could allow for balanced to unbalanced transitions, and the inherent directivity of the structure might also be used.

Appendix A

List of Publications

M. J. Cryan, P. R. Shepherd and S. R. Pennock, "Novel GaAs Monolithic Microwave Devices and Their Applications", *Proc. IEEE International Symposium on MMICs in Communication Systems*, King's College, London, September 1992.

M. J. Cryan, P. R. Shepherd and S. R. Pennock, "Modelling and Measurement of Wide FET Structures", *International Journal of Electronics*, Vol. 76, No.2, pp315-327, Feb. 1994.

M. J. Cryan, P. R. Shepherd and S. R. Pennock, "A Novel Voltage Controlled Directional Coupler Using a Wide FET Structure", *Proc. GAAS94 European Gallium Arsenide and Related III-V Compounds Applications Symposium*, Turin, Italy, April 1994.

M. J. Cryan, P. R. Shepherd and S. R. Pennock, "A Comparison of Three Wide FETs Configured as Controllable Couplers", *Proc. IEE Colloquium on Modelling, Design and Applications of MMICs*, London, June 1994.

M. J. Cryan, P. R. Shepherd and S. R. Pennock, "A Monolithic Voltage Controlled Directional Coupler", *Proc. 24^{th} European Microwave Conference*, Cannes, Sept. 1994.

INT. J. ELECTRONICS, 1994, VOL. 76, NO. 2, 315–327

Modelling and measurement of wide FET structures

M. J. CRYAN†, P. R. SHEPHERD† and S. R. PENNOCK†

A wide FET structure is considered as a voltage controlled directional coupler. A model for the device has been developed taking into account its distributed nature. The variation with bias of the source–drain *S*-parameters is presented and the model compares very well with measured results up to 20 GHz. The results show large variations in forward coupling from source to drain. The model has been used to investigate the effects of different gate terminations. Improved performance was then predicted and obtained, with 50 Ω loads. For this case the gate associated *S*-parameters are also presented.

1. Introduction

As GaAs monolithic microwave inegrated circuit (MMIC) technology has matured, there has been much interest in non-standard FET structures, where the flexibility of the MMIC process has been used to design novel devices. Wide FETs have been used as travelling wave FETs, where a growing wave propagates along the FET (D'Agostino *et al.* 1992), and a Schottky contact coplanar line has been used as a voltage controlled attenuator (Fleming *et al.* 1979).

In this work a wide FET has been configured as a four-port directional coupler, where the source, gate and drain lines can be considered as coupled microstrip transmission lines. The gate bias controls the amount of coupling between source and drain. A test structure has been fabricated through an SERC initiative and it has been shown (Cryan *et al.* 1992) that the coupling between the source and drain can be controlled by the gate bias over a large frequency range.

In this paper, we develop a theoretical model for the wide FET and compare the modelled results with measured results from the test structure. The model can then be used to obtain an optimum FET structure, given a particular specification.

2. Modelling

In order to understand the device operation and achieve improved performance, a model for the device has been constructed. The coupled mode method (D'Agostino *et al.* 1992, Tripathi 1975, 1977) is used to calculate the propagation characteristics of the device and from these the six-port scattering parameters (*S*-parameters) can be derived.

Initially, the static capacitances of the three electrodes are calculated. These have been evaluated using the resistive network analogue technique (Lennartsson 1972). This technique solves the laplacian finite difference problem by introducing suitably chosen resistors between the nodes of the finite difference mesh. Circuit theory is then

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used to obtain the resistance matrix for the air dielectric interface, where the conducting strips are present. Since only the potential of those nodes on the strips is of importance all other nodes can be omitted, giving a much reduced resistance matrix. This is then inverted, and the capacitances are found from this conductance matrix.

Under the quasi-TEM approximation, the self- and mutual inductances of the structure can be calculated from these static capacitances.

The model is then extended by adding the intrinsic FET parameters, C_{dep}, R_{dep} and R_{ds} (for $I_{ds}=0$) and the electrode resistances, R_g, R_d, and R_s as distributed elements shown in Fig. 1.

The series elements of the model, the inductances and electrode resistances, form the series impedance matrix for the structure, $[Z]$ and the parallel elements form the shunt admittance matrix, $[Y]$.

Having obtained the immitance parameters for the device, the propagation characteristics can be calculated using the coupled mode method (Tripathi 1975, 1977). The total voltages and currents on the lines are expressed using the standard telegrapher's equations, these can be written in matrix form as

$$-\frac{d[V]}{dz}=[Z][I] \tag{1}$$

$$-\frac{d[I]}{dz}=[Y][V] \tag{2}$$

Differentiating (1) with respect to z, substituting in (2) and assuming the form of V to be $V=V_0\exp(-\gamma z)$, a standard solution to this type of problem, where γ is the propagation constant, we obtain (3):

$$\gamma^2[V]=[Z][Y][V] \tag{3}$$

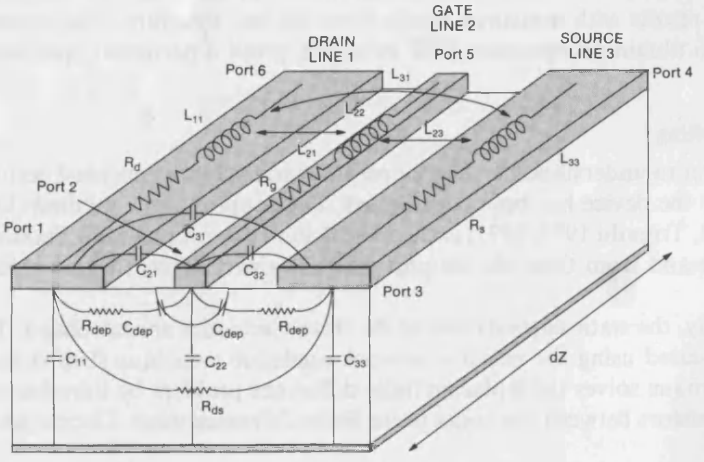


Figure 1. Unit cell for the distributed model of a wide FET structure.

Where γ^2 is the eigenvalue of the equation. The solution of this standard problem produces three eigenvalues which give three propagation constants, each representing a different mode of propagation for the three-line system, these will be denoted *a*, *b* and *c*. From these eigenvalues, eigenvectors are obtained which are the voltage solutions for each of the modes and it can be shown that they have forward and backward wave components. The total voltage on line 1 of the system, obtained by superimposing the three modes, is

$$V_1 = A_{1a} \exp(-\gamma_a z) + A_{2a} \exp(+\gamma_a z) + A_{1b} \exp(-\gamma_b z)$$
$$+ A_{2b} \exp(+\gamma_b z) + A_{1c} \exp(-\gamma_c z) + A_{2c} \exp(+\gamma_c z) \quad (4)$$

The eigenvectors from (3) interrelate the mode voltages on each of the lines: if they are normalized with respect to the mode voltages of line 1, the total voltages for the three lines can be written in matrix form

$$[V] = [R_v][[A_1] + [A_2]] \quad (5)$$

Where $[V]$ is the 3×1 matrix of total voltages, $[R_v]$ is the 3×3 matrix of normalized eigenvectors and $[A_1]$ and $[A_2]$ are the 3×1 matrices of phasor voltage amplitudes of the forward and backward waves on line 1 for the three modes.

Defining mode admittance as the ratio of mode current to mode voltage, we can write

$$[I] = [[R_v] \bullet [Y^m]][[A_1] - [A_2]] \quad (6)$$

Where $[I]$ is the 3×1 matrix of total currents, $[Y^m]$ is the 3×3 matrix of mode admittances, $[A_1]$ and $[A_2]$ are the 3×1 matrices of voltage mode amplitudes, the negative sign of the backward wave is required if this is to be a solution of equations (1) and (2) and $\bullet$ implies multiplication of the individual elements of the matrix, i.e. if $[c] = [a] \bullet [b]$, then $c_{11} = a_{11} * b_{11}$. If (6) is differentiated with respect to z, then we obtain

$$\frac{d[I]}{dz} = -[[R_v] * [Y^m]][\gamma][A_1 + A_2] \quad (7)$$

where $[\gamma]$ is the 3×3 diagonal matrix of propagation constants.

If (7) and (5) are substituted in (2), equation (8) is obtained:

$$[R_v] * [Y^m][\gamma] = [Y] * [R_v] \quad (8)$$

Expressions for $[Y^m]_{ij}$ can now be written, and since each mode on each line is now expressed independently, not in the coupled form of (3), the mode impedance is simply the inverse of the mode admittance, $[Z^m]_{ij} = 1/[Y^m]_{ij}$, the expressions are given in Appendix A.

The propagation characteristics of the FET have been derived, these are now used in a modal analysis, outlined below, which yields scattering parameters (*S*-parameters) for the six-port FET structure (Tripathi 1981). Each of the three lines is now treated as an uncoupled line with its own propagation characteristics. Firstly, we need to define the reflection (Γ) and transmission (T) coefficients for each mode

on each line. These are given by Rizzi (1988) as

$$\Gamma_{xk}=\frac{\left(\frac{Z_{xk}}{Z_k}-\frac{Z_k}{Z_{xk}}\right)\sinh(\gamma_x l)}{2\cosh(\gamma_x l)+\left(\frac{Z_{xk}}{Z_k}-\frac{Z_k}{Z_{xk}}\right)\sinh(\gamma_x l)} \tag{9}$$

$$T_{xk}=\frac{2}{2\cosh(\gamma_x l)+\left(\frac{Z_{xk}}{Z_k}-\frac{Z_k}{Z_{xk}}\right)\sinh(\gamma_x l)} \tag{10}$$

Where x denotes the mode a, b or c, k line 1, 2 or 3, Z_{xk}^m the mode impedance and Z_k the line terminating impedance. The terminating impedances are chosen such that the reflection coefficients for each mode are equal, for each of the three lines. These are referred to as non-mode-converting (NMC) terminations (Gunton and Paige 1978). These terminations ensure that when a mode is incident upon the terminations, the reflected and incident wave are of the same mode. The S-parameters will then be referenced to these NMC terminations, but they could be referenced to the standard 50 Ω using the theory outlined by Tripathi (1982). The S-parameters are then defined by choosing amplitudes for the three modes such that unity power wave is incident upon port 1 of the six-port structure. The expressions for the S-parameters of the general symmetrical three-line structure are given in Appendix B.

3. Measured and modelled results

The FET chip measures 2·0 mm × 1·0 mm × 0·2 mm and is mounted on a brass pedestal with tape bonds connecting the terminals of the source and drain lines to incoming microstrip lines. Bias voltage is applied to the gate line via a choke coil; i.e. the gate connections are initially modelled as open circuits. The multiport connection method (Gupta *et al.* 1981) has been used to include the effect of the tape bonds by adding two-port networks to the basic six-port FET structure. The results from the multiport connection method agree exactly with those obtained from passing the six-port S-parameter block to EEsof™ and adding external inductances.

Measured and modelled results are shown in Fig. 2 for three different gate bias levels: 0 V, −1·59 V and −2·5 V. Initially, the FET parameters were based on those given by Ayalsi (1982) and then optimized to give the best fit; R_g, R_s and R_d were obtained by DC resistance measurement. R_{dep} has been assumed to be constant with bias. The dimensions of the FET are: coupled length = 1·5 mm, source length = drain length = 38 μm, gate length = 1 μm, source-gate spacing = drain-gate spacing = 2·3 μm and substrate thickness = 200 μm. C_{dep} and R_{dep} were set for each bias level, C_{dep} = 0·90, 0·47, 0·13 pF and R_{ds} = 6 Ω, 200 Ω, 60 kΩ for 0 V, −1·59 V, −2·5 V, respectively, R_g = 150 Ω, $R_s = R_d$ = 1·13 Ω and R_{dep} = 2·0 Ω.

There is good agreement between the measured and the modelled data. All the trends and magnitudes are reproduced well up to 20 GHz. These results show very little variation in reverse coupling, S_{21}, but much larger variation in forward coupling, S_{41}, which reduces to −20 dB from 4 to 8 GHz, at pinch-off. The results at pinch-off are similar to the classical two line microstrip backward wave coupler.

Thus the device would seem to have two limiting states: (i) *zero bias*—the channel resistance is low $\simeq 6\,\Omega$ and there is an equal power split between ports 3 and 4, with slightly higher coupling to port 2; (ii) *pinch-off*—the structure behaves as a set of coupled lines on a lossless substrate, with port 3 isolated, port 4 the through-line and port 2 the backward coupled port.

Having developed a good model for the device, the effect of different gate terminations was investigated in order to improve the isolation of the forward coupled port and thus increase the amount of variation in the transmission to this port. Using the model, various terminations were placed at either end of the gate line; the most interesting results were obtained with $50\,\Omega$ loads. This was then carried out experimentally using external loads connected to the gate via microstrip lines, with DC blocking capacitors to prevent the loads drawing high currents and damaging the gate line, these results are shown in Fig. 3. The model agrees very well with measured results and the level of S_{41} has decreased from around $-20\,\text{dB}$ to $-28\,\text{dB}$ from 4–6 GHz. Thus we have shown it is possible to obtain large variation in the coupling between ports 1 and 3 and ports 1 and 4 of the device, whilst maintaining relatively constant coupling in the reverse direction to port 2.

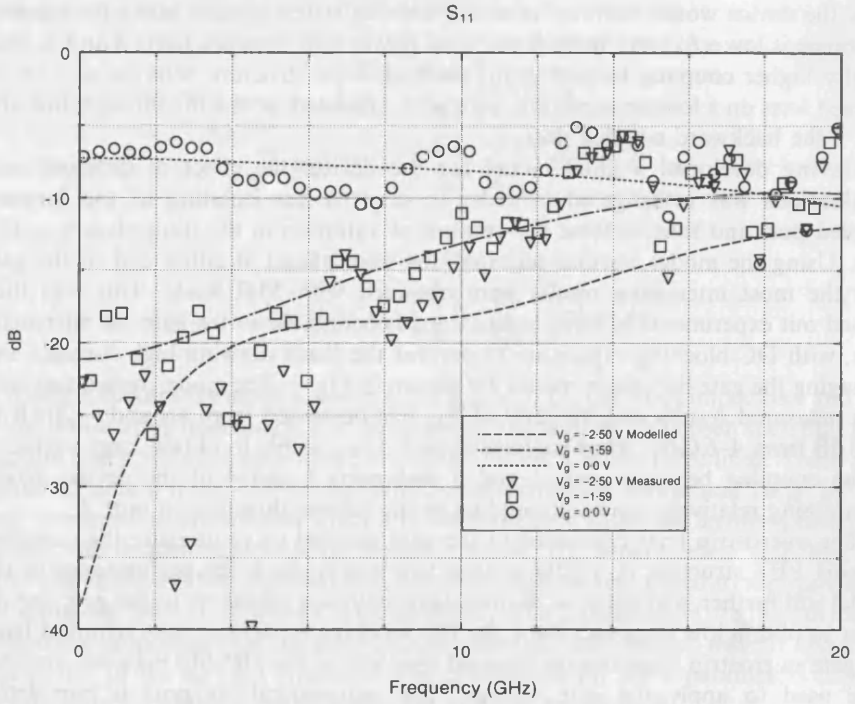
The microstrip lines connected to the gate enabled us to measure the complete six-port FET structure in a $50\,\Omega$ system, this would check the performance of the model still further, and allow us to investigate coupling effects on to the gate line. In order to obtain low frequency data, the DC blocking capacitors were removed from the gate microstrip lines and the internal bias tees of the HP8510 network analyser were used to apply the gate voltage. The symmetrical six port is completely characterized by eight S-parameters; four have been shown previously, the additional four associated with the gate are shown in Fig. 4. Again, good agreement is obtained and similar performance to the drain–source coupling is observed, with relatively constant reverse coupling S_{21} and large variation in the forward coupling S_{51}. The insertion loss of the gate, S_{52}, is quite high owing to the high DC series resistance caused by the small cross-sectional area of the gate.

4. Conclusion

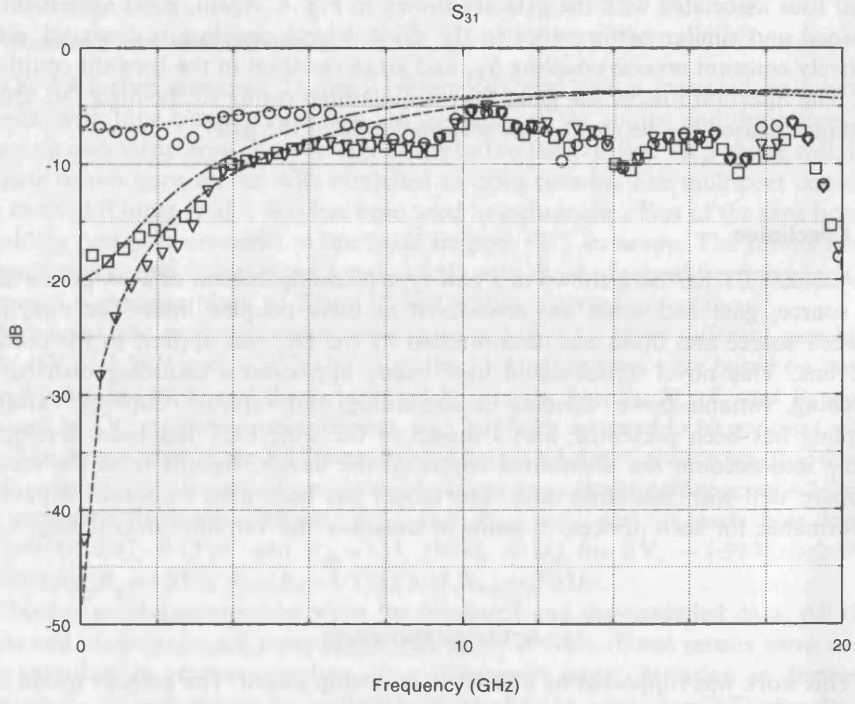
A wide FET has been shown in a new type of configuration, as a six-port where the source, gate and drain are considered as three coupled lines. The coupling between source and drain can be controlled by the DC bias applied to the central gate line. This novel device could have many applications including distributed switching, variable power dividing or combining, and variable coupling. Variable coupling has been presented, and a model of the wide FET has been developed taking into account the distributed nature of the device. Results from the model compare well with measured data. The model has been used to obtain improved performance for such devices, in terms of isolation and variation in coupling.

ACKNOWLEDGMENTS

This work was supported by a SERC studentship award. The authors would like to thank Trevor Ryan for mounting the MMICs in the microstrip measurement fixtures.


S11
0
-10
-20
-30
-40
dB
0
10
20
Frequency (GHz)
Vg = -2·50 V Modelled
Vg = -1·59
Vg = 0·0 V
Vg = -2·50 V Measured
Vg = -1·59
Vg = 0·0 V

2(*a*)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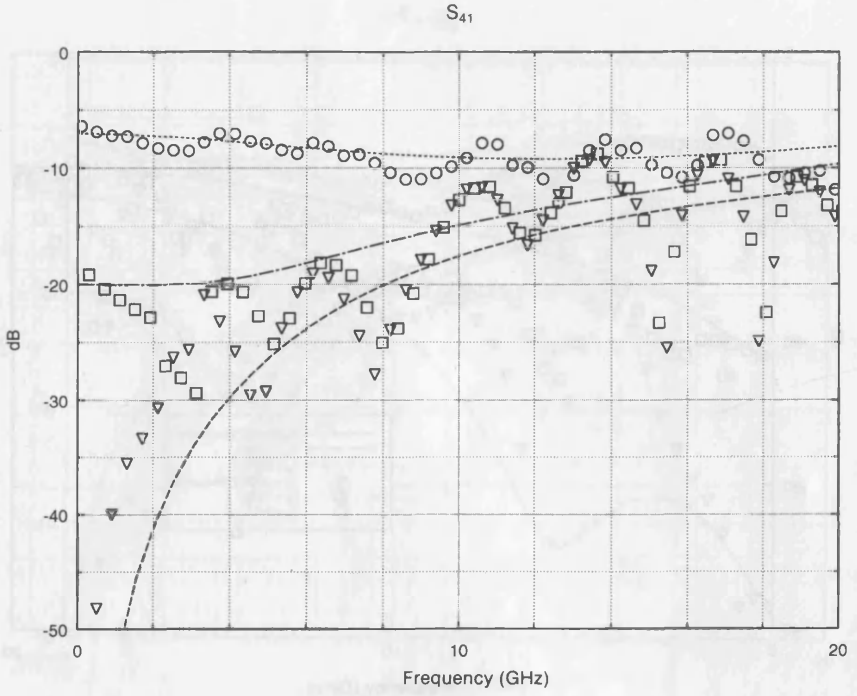
-10
-20
-30
-40
-50
dB
0
10
20
Frequency (GHz)

2(*b*)



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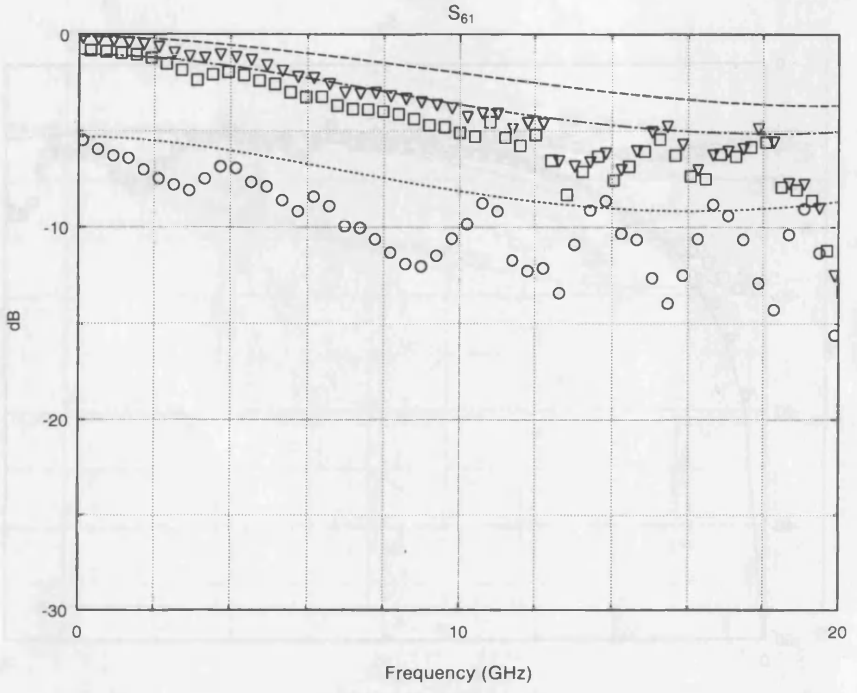
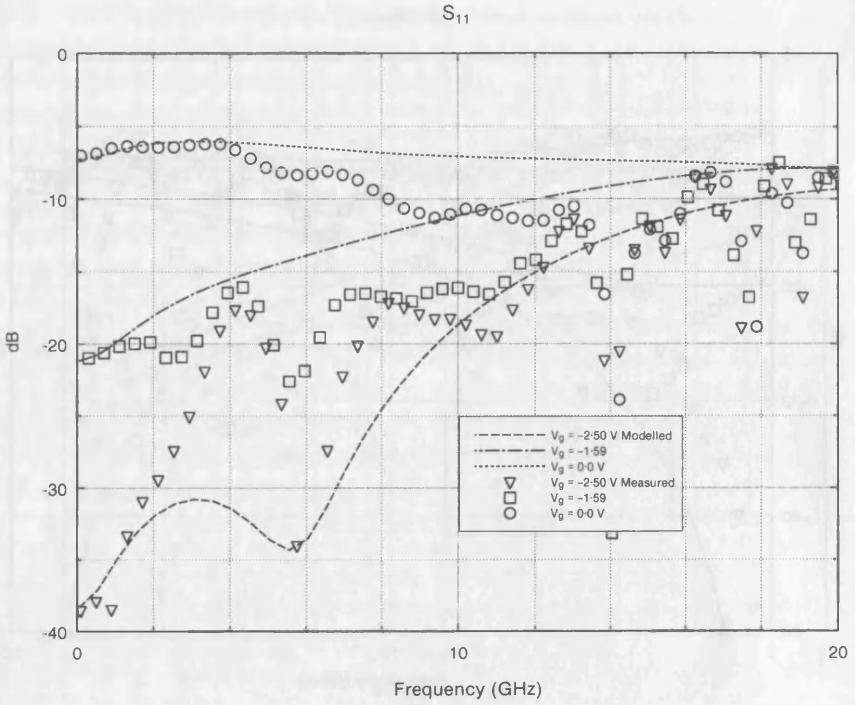


(*d*)

Figure 2. *S*-parameters of a wide FET structure for different gate bias levels with an open circuited gate.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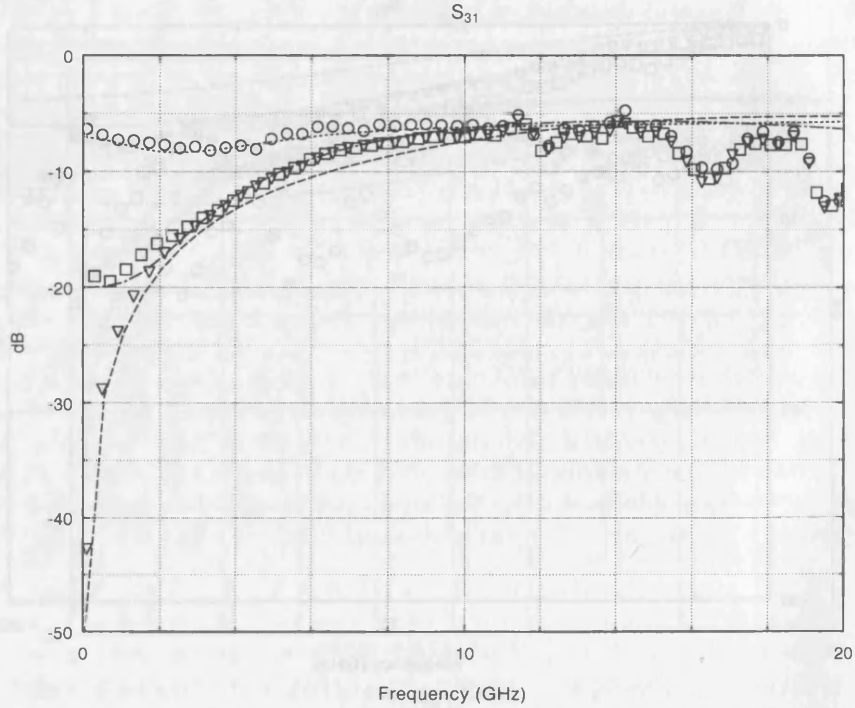
0
-10
-20
-30
-40
dB
0
10
20
Frequency (GHz)
Vg = -2·50 V Modelled
Vg = -1·59
Vg = 0·0 V
Vg = -2·50 V Measured
Vg = -1·59
Vg = 0·0 V

3(*a*)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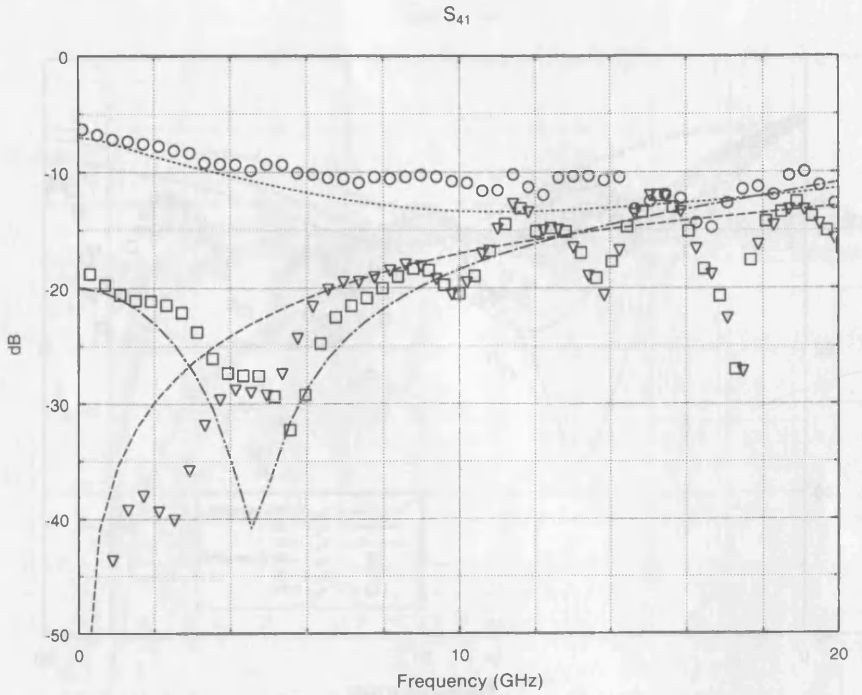
0
-10
-20
-30
-40
-50
dB
0
10
20
Frequency (GHz)

3(*b*)



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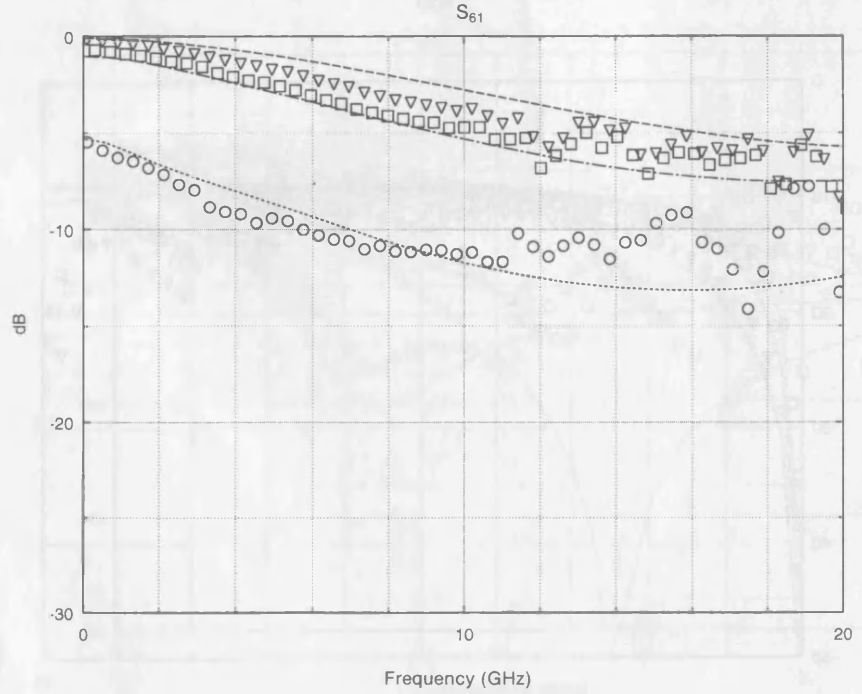
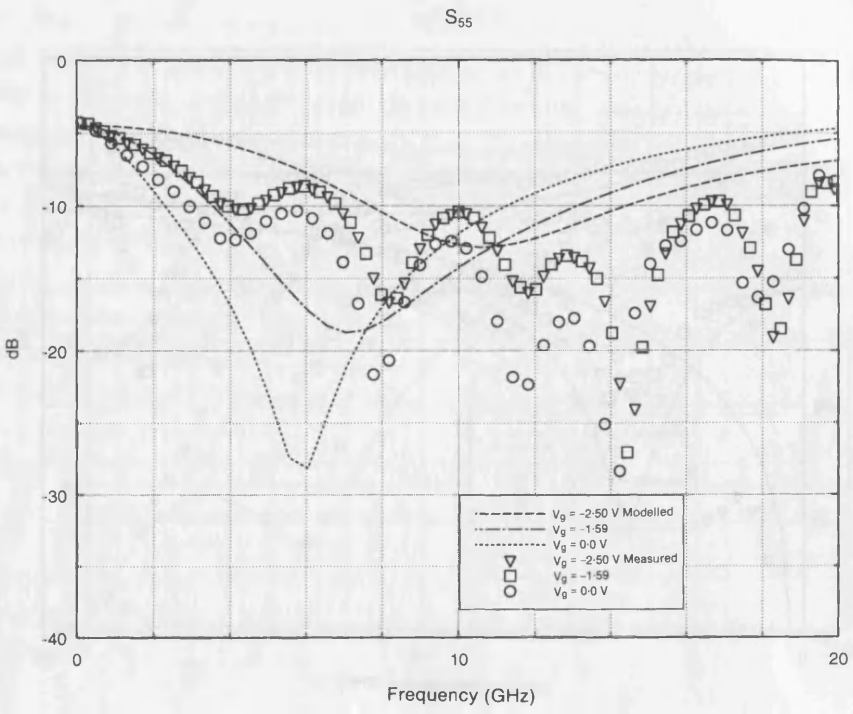
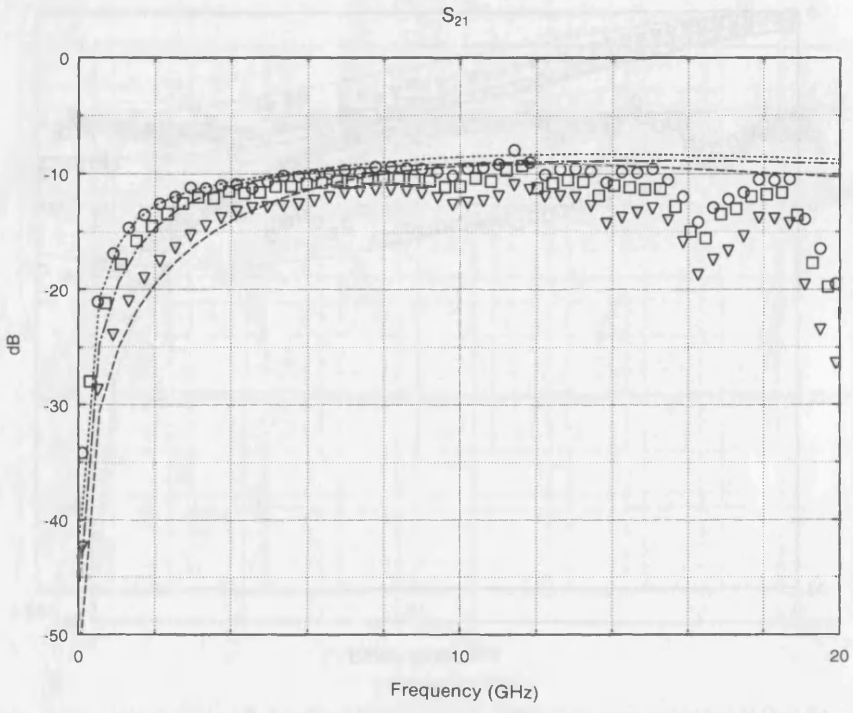


(*d*)

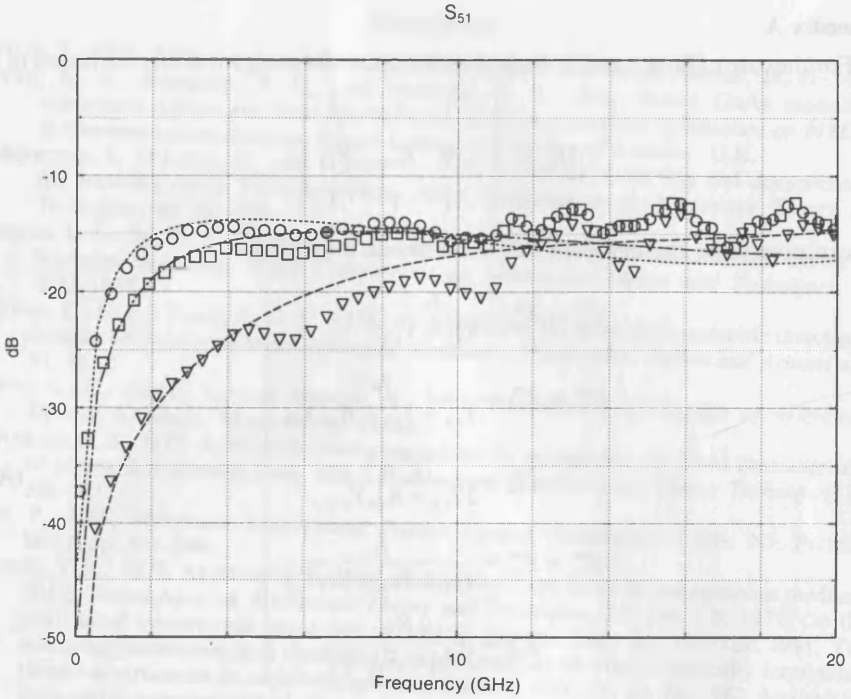
Figure 3. *S*-parameters of a wide FET structure for different gate bias levels with a 50 Ω terminated gate.


S55
0
-10
-20
-30
-40
dB
0
10
20
Frequency (GHz)
Vg = -2·50 V Modelled
Vg = -1·59
Vg = 0·0 V
Vg = -2·50 V Measured
Vg = -1·59
Vg = 0·0 V

4(*a*)


S21
0
-10
-20
-30
-40
-50
dB
0
10
20
Frequency (GHz)

4(*b*)



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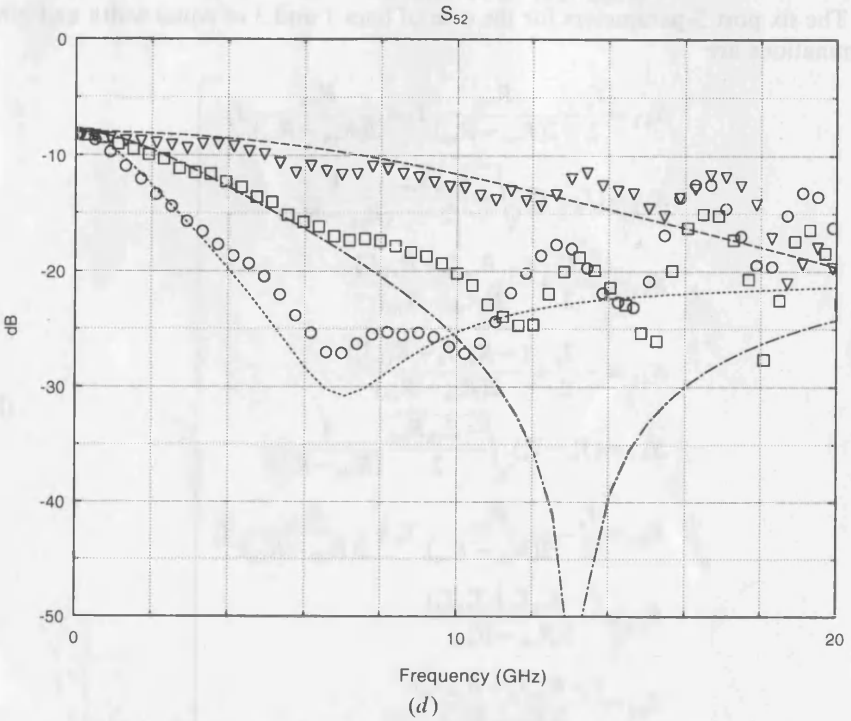

(*d*)

Figure 4. Gate associated *S*-parameters of a wide FET structure for different gate bias levels with a 50 Ω terminated gate.

Appendix A

For the case of lines 1 and 3 of equal width, the voltage eigenvectors are found to be

$$[R_v] = \begin{bmatrix} 1 & 1 & 1 \\ 0 & R_{vb} & R_{vc} \\ -1 & 1 & 1 \end{bmatrix} \tag{A 1}$$

we can now write the expressions for the mode impedances

$$\left.\begin{aligned} Z_{a1}^m = Z_{a3}^m &= \frac{\gamma_a}{Y_{11} - Y_{13}} \\ Z_{b1}^m = Z_{b3}^m &= \frac{\gamma_b}{Y_{11} + Y_{13} + R_{vb} Y_{12}} \\ Z_{b2}^m &= \frac{\gamma_b R_{vb}}{2Y_{12} + R_{vb} Y_{22}} \\ Z_{c1}^m = Z_{c3}^m &= \frac{\gamma_c}{Y_{11} + Y_{13} + R_{vc} Y_{12}} \\ Z_{c2}^m &= \frac{\gamma_c R_{vc}}{2Y_{12} + R_{vc} Y_{22}} \end{aligned}\right\} \tag{A 2}$$

Appendix B

The six port S-parameters for the case of lines 1 and 3 of equal width and NMC terminations are

$$\left.\begin{aligned} S_{11} &= \frac{\Gamma_a}{2} - \frac{R_{vc}}{2(R_{vc} - R_{vc})} \Gamma_b + \frac{R_{vb}}{2(R_{vb} - R_{vc})} \Gamma_c \\ S_{21} &= (\Gamma_b - \Gamma_c) \sqrt{\frac{-R_{vb} R_{vc}}{2}} \frac{1}{(R_{vb} - R_{vc})} \\ S_{31} &= -\frac{\Gamma_a}{2} + \frac{(-R_{vc} \Gamma_b + R_{vb} \Gamma_c)}{2(R_{vb} - R_{vc})} \\ S_{41} &= -\frac{T_a}{2} + \frac{(-R_{vc} T_b + R_{vb} T_c)}{2(R_{vb} - R_{vc})} \\ S_{51} &= (T_b - T_c) \sqrt{\frac{-R_{vb} R_{vc}}{2}} \frac{1}{(R_{vb} - R_{vc})} \\ S_{61} &= \frac{T_a}{2} - \frac{R_{vc}}{2(R_{vb} - R_{vc})} T_b + \frac{R_{vb}}{2(R_{vb} - R_{vc})} T_c \\ S_{22} &= \frac{(-R_{vc} \Gamma_c + T_{vb} \Gamma_b)}{2(R_{vb} - R_{vc})} \\ S_{52} &= \frac{(-R_{vc} T_c + R_{vb} T_b)}{2(R_{vb} - R_{vc})} \end{aligned}\right\} \tag{B 1}$$

All other S-parameters can be derived from these using symmetry.

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A Novel Voltage Controlled Directional Coupler Using A Wide FET Structure

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Abstract

A wide FET is considered as a voltage controlled directional coupler. A model for the device has been developed taking into account the distributed nature of the device. The six port measured and modelled S-parameters are shown to 20GHz. The results show large variation in coupling between source and drain.

Introduction

As MMIC technology has matured there has been much interest in non-standard FET structures, where the flexibility of the MMIC design process has been used to design novel devices. Wide FET's have been used as travelling wave FETs, where a growing wave propagates along the FET [1] and a Schottky contact coplanar line has been used as a voltage controlled attenuator [2]. In this work a wide FET has been configured as a four port directional coupler, where the source, gate and drain lines can be considered as coupled microstrip transmission lines and the gate bias controls the amount of coupling between source and drain. A test structure has been fabricated with a coupled length of 1.5mm and it has been shown [3] that the coupling between the source and drain can be controlled over a large frequency range. A typical wide FET structure is shown in figure 1, this chip measures 1.0mm x 3.0mm. A theoretical model of the wide FET has been developed taking into account the distributed nature of the device and the parasitics associated with mounting the device have also been included. The modelled results are compared with measured results from the test structure and good agreement has been obtained. The model has been used to investigate the effects of different gate terminations, improved performance was predicted, and has been obtained, with 50Ω loads.

Modelling

In order to understand the device operation and achieve improved performance, a model for the device has been constructed. The coupled mode method, [1], [4] is used to calculate the propagation characteristics of the device and from these the six-port Scattering parameters (S-parameters) can be derived. Firstly the static capacitances of the three electrodes are calculated. These have been evaluated using the resistive network analogue technique [5]. This technique solves the Laplacian finite difference problem by introducing resistors between the nodes of the finite difference mesh. If conducting strips are introduced into the resistive mesh, it can be shown [5] that the sum of the currents flowing into the nodes occurring on the strips is proportional to the charge density at that point. The sum of all strip node currents gives the total charge on the strip and hence the capacitance can be found. Under the Quasi-TEM approximation, the self and mutual inductances of the structure can be calculated from the static capacitances. The model is then extended by adding the intrinsic FET parameters, C_{dep}, R_{dep} and R_{ds} as distributed elements (@ I_{ds}=0). A diagram of the FET model is shown in fig. 2. The distributed immittance parameters are derived for the device and the propagation characteristics can be calculated using the coupled mode method. This analysis shows that such a three-line structure supports three possible modes, each having its own complex propagation constant. A mode impedance for each of the modes, on each of the lines is then calculated. These propagation characteristics are then used in a modal analysis which yields the scattering parameters for the six port FET structure.

Measured and Modelled Results

The FET chip measures 2.0mm x 1.0mm x 0.2mm and is mounted on a brass pedestal with tape bonds connecting the terminals to incoming microstrip lines. Initially dc was applied to the gate line via a bias resistor mounted in a high impedance line. These results are shown in fig. 3, it can be seen that at zero bias, when the channel resistance is low, the power incident on the source line splits equally between the output of the source line , S_{61} and the forward coupled port of the drain line, S_{41}, with slightly higher coupling to the backward coupled port of drain line, S_{31}. At pinch off the device acts as a set of coupled lines on a low loss substrate, with the output of the source as the through line and the drain line exhibiting backward coupling and forward isolation. The modelled results were found to agree very well with the measured results up to 20GHz. The model was then

used to find the gate terminations that resulted in the largest variation in forward coupling to the drain, these were found to be 50Ω loads. External 50Ω loads were then connected to the gate line via microstrip transmission lines and the results are shown in fig. 4. The forward transmission to the drain line , S_{41} is seen to be reduced by approximately 5dB at $V_g = -1.5V$ from 4 to 6GHz. S_{31} is slightly reduced, but still remains relatively constant. Thus an improvement in the isolation of the source and drain lines has been obtained with the addition of 50Ω loads. The transmission lines attached to the gate line have allowed the gate associated S-parameters to be measured. These are shown in fig. 5, directional coupling is again observed and they show good agreement between measured and modelled results. Thus the model shows good agreement for all eight S-parameters required to fully describe a symmetrical six port.

Conclusion

A wide FET has been shown in a new type of configuration, as a six port where the source, gate and drain are considered as three coupled lines. The coupling between source and drain can be controlled by the d.c. bias applied to the central gate line. This novel device could have many applications including distributed switching, variable power dividing or combining, variable coupling and variable phase shifters. Variable coupling has been presented, and a model of the wide FET has been developed taking into account the distributed nature of the device. Results from the model compare well with measured data. The model has been used to obtain improved performance for such devices, in terms of isolation and variation in coupling.

References

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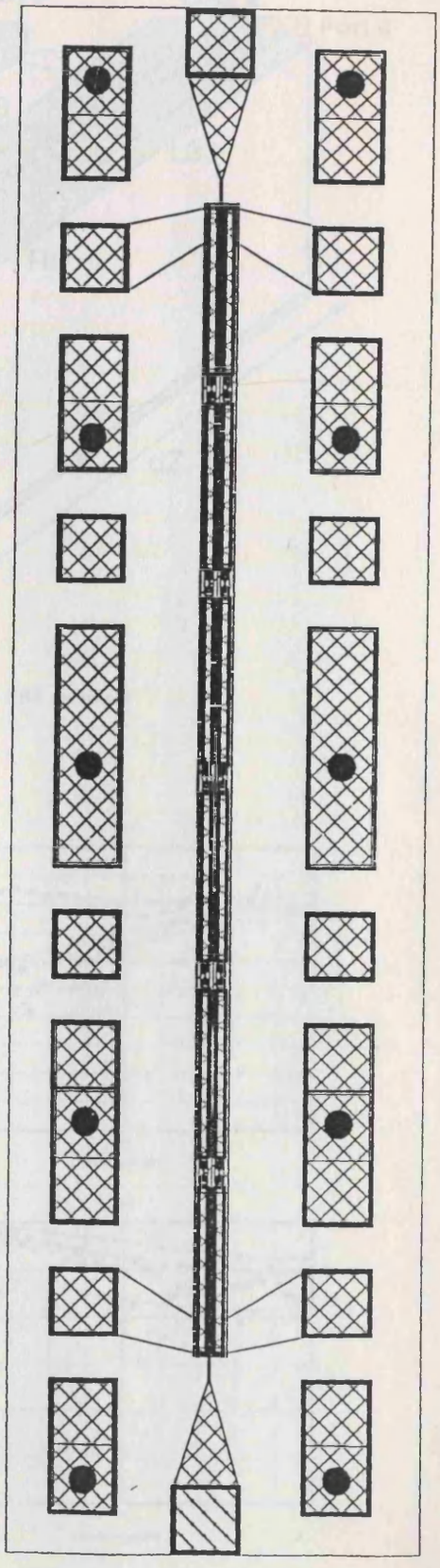

Fig 1. A wide FET structure

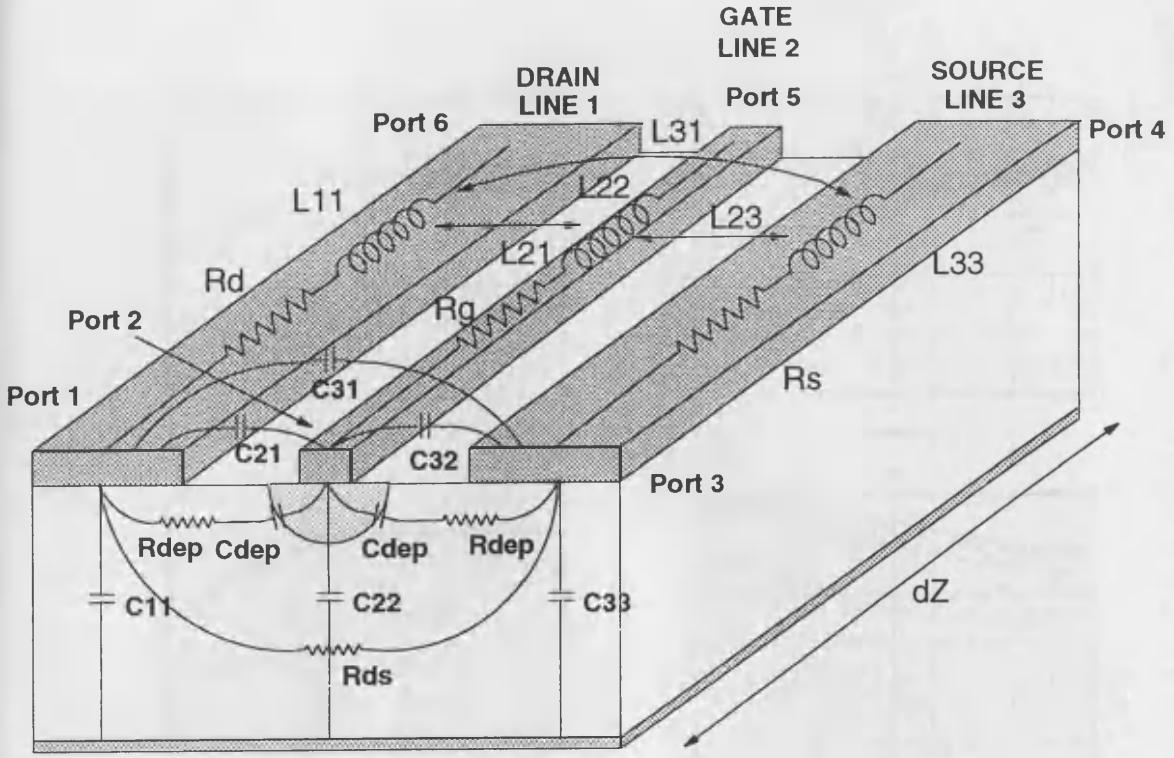

Fig 2. Unit cell for the distributed model of a wide FET structure

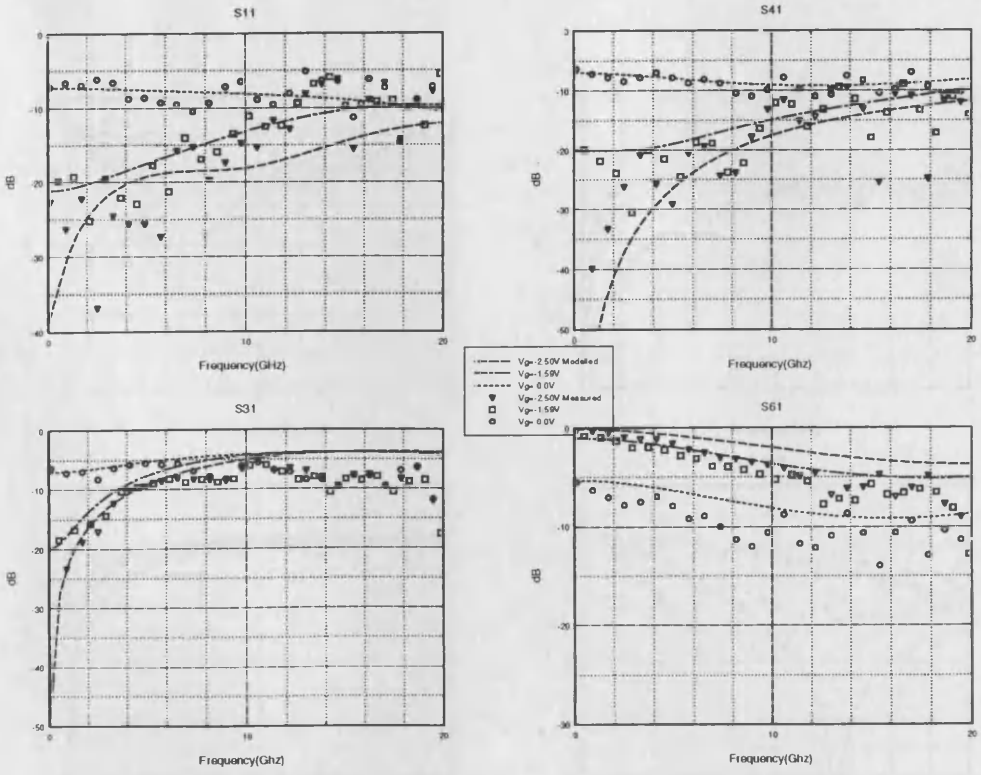

Fig 3. Measured and modelled source-drain associated S-parameters for a wide FET with an open circuited gate line.

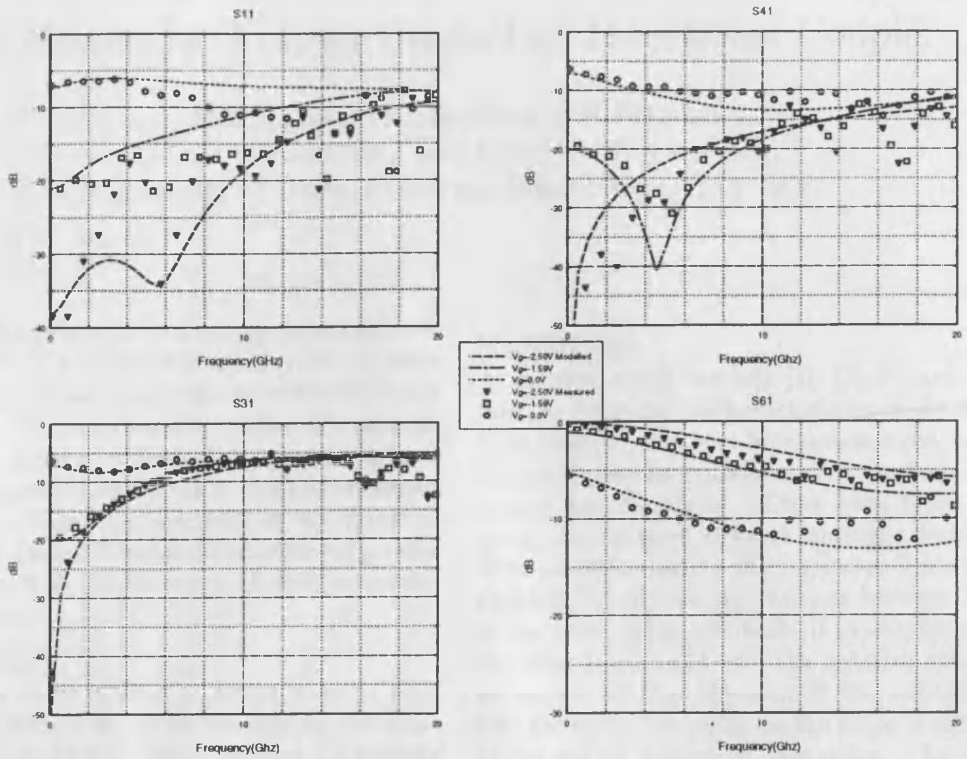

Fig 4. Measured and modelled source-drain associated S-parameters for a wide FET with 50Ω terminated gate line.

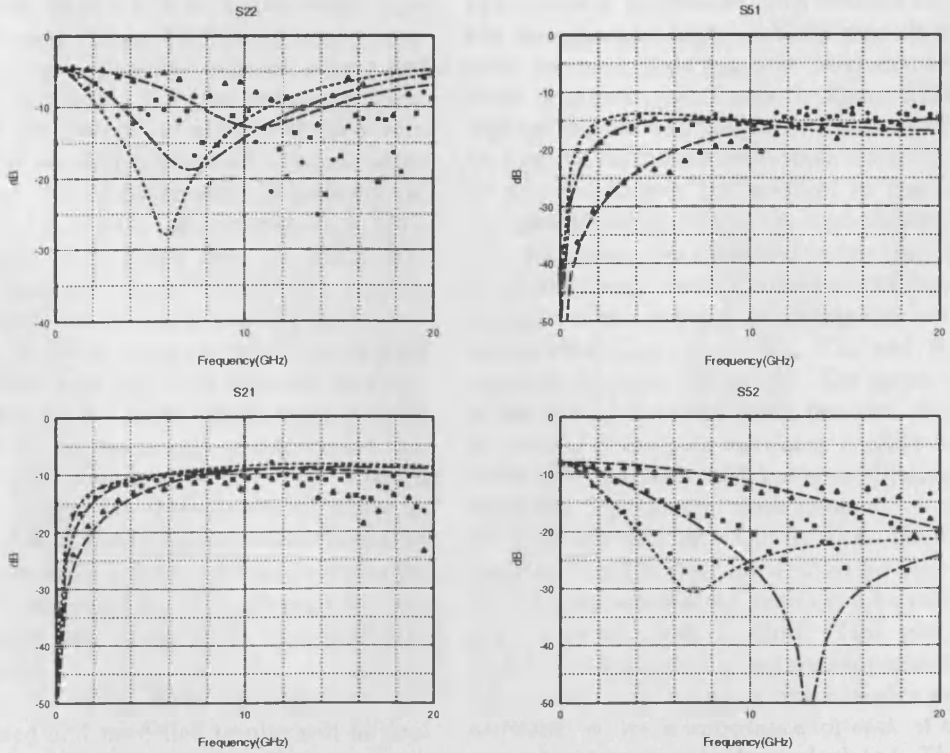

Fig 5. Measured and modelled gate associated S-parameters for a wide FET with 50Ω terminated gate line.

A Monolithic Voltage Controlled Directional Coupler

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ABSTRACT

A wide FET is considered as a voltage controlled directional coupler. A model for the device has been developed taking into account the distributed nature of the device. Measured and modelled six port S-parameters for three such devices are presented from 0.1-20GHz. Directional coupling is observed between source and drain lines, the directivity of which is tunable by d.c. gate bias. Tunable directivities of greater than 20dB from 6 to 12GHz are predicted for the de-embedded device.

INTRODUCTION

There has been much interest in recent years in non-standard FET structures, made feasible by the flexibility of the GaAs MMIC design process. Travelling wave FETs that are 1.2mm wide have been fabricated, here a growing wave propagates down the device, giving very broadband gain [1] and Schottky contact coplanar line has been used as a voltage controlled attenuator [2].

In this work three wide FETs with different widths and electrode dimensions are configured as six ports. Directional coupling is observed between source and drain lines, gate and drain, and gate and source lines. As in standard microstrip couplers backward coupling and forward isolation is observed. The variation of the six port scattering parameters (S-parameters) for each device are shown for different gate bias, from 0.1GHz to 20GHz. It is found that, for the source and drain lines, once the channel resistance is reasonably high, $> 100\Omega$, the forward coupling and insertion loss remain relatively constant, while the forward isolation is tunable with gate bias, thus the directivity of the coupler can be tuned. Such devices could find application within microwave measurement systems where coupler directivity is often the limiting factor on performance. On-chip tunability would be extremely desirable in MMIC applications where very tight specifications are required or where process variation needs to be corrected for. The tuning voltage is applied only to the gate of the FET, thus negligible power is consumed.

A theoretical model of the wide FET has been developed, measured and modelled results will be presented showing good agreement for all three structures. This model can be used to obtain optimum device geometries for a given coupler specification.

MODELLING

A coupled mode method [1], [3] is used to calculate the propagation characteristics of the device and from these the six-port S-parameters can be derived. Firstly the static capacitances of the four conductor system are calculated. These have been evaluated using the resistive network analogue technique [4]. This technique solves the Laplacian finite difference problem by introducing resistors between the nodes of the finite difference mesh. If the conducting strips are then introduced into the resistive mesh, it can be shown [4] that the sum of the currents flowing into the nodes occurring on the strips is proportional to the charge density at that point. The sum of all strip node currents gives the total charge on the strip and hence the capacitance can be found. Since only the currents and voltages on the strips are of interest the size of matrix to be inverted in order to evaluate the currents is dramatically reduced, normally by two orders of magnitude, thus considerably reducing the computation time. Initially zero thickness lines were assumed, this has now been extended to the finite thickness case. Under the Quasi-TEM approximation, the self and mutual inductances of the structure can be calculated from these static capacitances. These capacitances are modified by the presence of the gate depletion region; the depletion region masks the capacitance between source-gate and drain-gate, thus only the air path capacitances are included. The model is then extended by adding the intrinsic FET parameters, C_{dep}, R_{dep}, R_{ds}, C_{ds} and R_{n+} as distributed elements (@ I_{ds}=0). The series resistances of the source, gate and drain lines are also included. In particular the gate resistance is quite high, of the order of 100KΩ/m, which has been obtained from low frequency S-parameter measurements. A diagram of the FET model is shown in figure 8. The distributed immitance parameters are derived for the device and the propagation characteristics can be calculated using a coupled mode method. This analysis shows that such a three-line structure supports three possible modes, each having its own complex propagation constant. A mode impedance for each of the modes, on each of the lines, is then calculated. These propagation characteristics are then used in a modal analysis which yields the scattering parameters for the

six port FET structure. This analysis is described in more detail by the authors in [5]. The effect of the external tape bonds has been modelled using the multiport connection method, in which inductances are added in series to each of the six ports enabling the embedded S-parameters to be calculated.

RESULTS.

The devices have been fabricated on 200μm GaAs through the Eurochip programme at GEC MMT Ltd. The FET's have three different geometries:- FET 1: width = 1.33mm, source = drain length = 94μm; FET 2: width = 1.50mm, source = drain length = 38μm; FET 3: width = 2.00mm, source = drain length = 22μm. The chips are mounted on a brass pedestal with tape bonds connecting the terminals to incoming microstrip lines. The gate line is also connected to microstrip lines, enabling full six port characterisation of the device. Measured and modelled results are shown in figures 1 - 6 and show good agreement. The three devices exhibit the same general behaviour : in the zero bias state the power incident on the source line splits equally between the source and drain outputs, with slightly higher backward coupling to the drain input ; as the reverse bias on the gate increases, the channel resistance increases and the source and drain lines begin to act as a set of coupled lines on a low loss substrate. The backward coupling, S_{31} increases with increasing electrode length, for FET 3 at 10GHz S_{31}=-5dB, for FET 2 S_{31}=-6dB and for FET 1 S_{31}=-8dB, this trend agrees with that of passive coupled microstrip lines. The effect of electrode width is also observed, FET 1, the widest FET, shows the lowest frequency of maximum backward coupling. The main feature of interest is the tunable resonance observed in the forward isolation, S_{41}, this is at a maximum for FET 3 at -40dB, this corresponds to a directivity of greater than 30dB. The resonance can be tuned across a 2-3GHz band with little change in backward coupling, return loss or insertion loss. In FETs 1 and 2 the resonance is observed to be much lower Q. The gate associated S-parameters have been measured and modelled and also show good agreement. Directional coupling is again observed, with much lower directivities and less tunability. The effect of high gate resistance is seen in the low level of S_{52} at low frequency.

The model was then used to predict the de-embedded performance of the FET, with the effect of the external tape bonds reduced, from 0.3nH to 0.05nH. This is more representative of the connection inductance if the FET was integrated into a system on chip. The results for FET 2 are shown in figure 7. There is as marked improvement in all the coupler's key parameters. The return loss has been reduced to $\simeq -15$dB across the whole band, the insertion loss has been reduced from 4-6dB to 3-5dB @ 10GHz, whilst the backward coupling has remained unchanged and as expected the isolation has improved substantially. This simulation predicts a directivity of greater than 20dB from 6 to 12GHz, moreover it is tunable within this band. This simulation highlights the difficulties inherent in measuring four port devices, even with on-wafer probing; reflections from terminated ports lead to inaccuraccies and it is hoped that with the use of on chip terminations, the intrinsic performance of the device can be measured.

CONCLUSION.

A wide FET has been shown in a new type of configuration, as a six port where the source, gate and drain are considered as three coupled lines. The forward isolation and hence the directivity between source and drain can be controlled by the d.c. bias applied to the central gate line. Three such devices have been fabricated and characterised, a model has been developed for the wide FET and the modelled results show good agreement with measured data. This novel device could have many applications including variable directivity couplers, variable power dividing or combining, distributed switching and variable phase shifters. The model developed has been used to predict the de-embedded performance of the FET without the influence of tape bond connections, very high, tunable directivities are predicted. Using the developed model the FET geometry for optimum coupler performance in terms of isolation and coupling over a given frequency range, can now be obtained.

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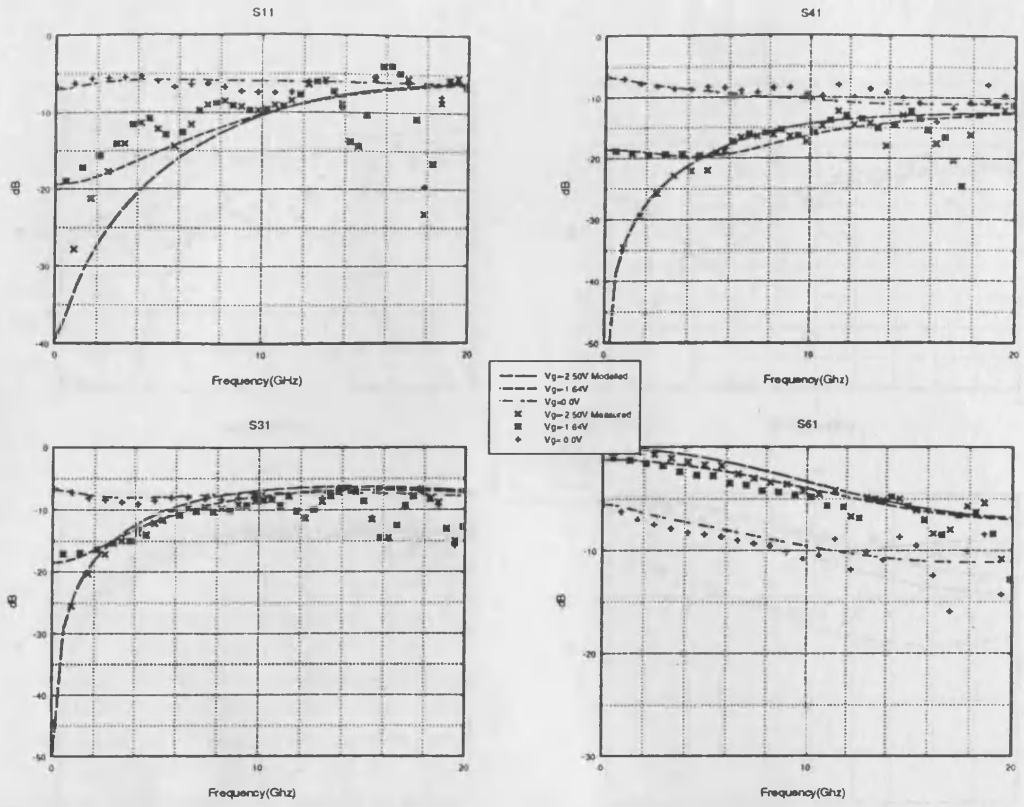

Fig 1. Measured and modelled source-drain S-parameters for a wide FET with 94μm source length.

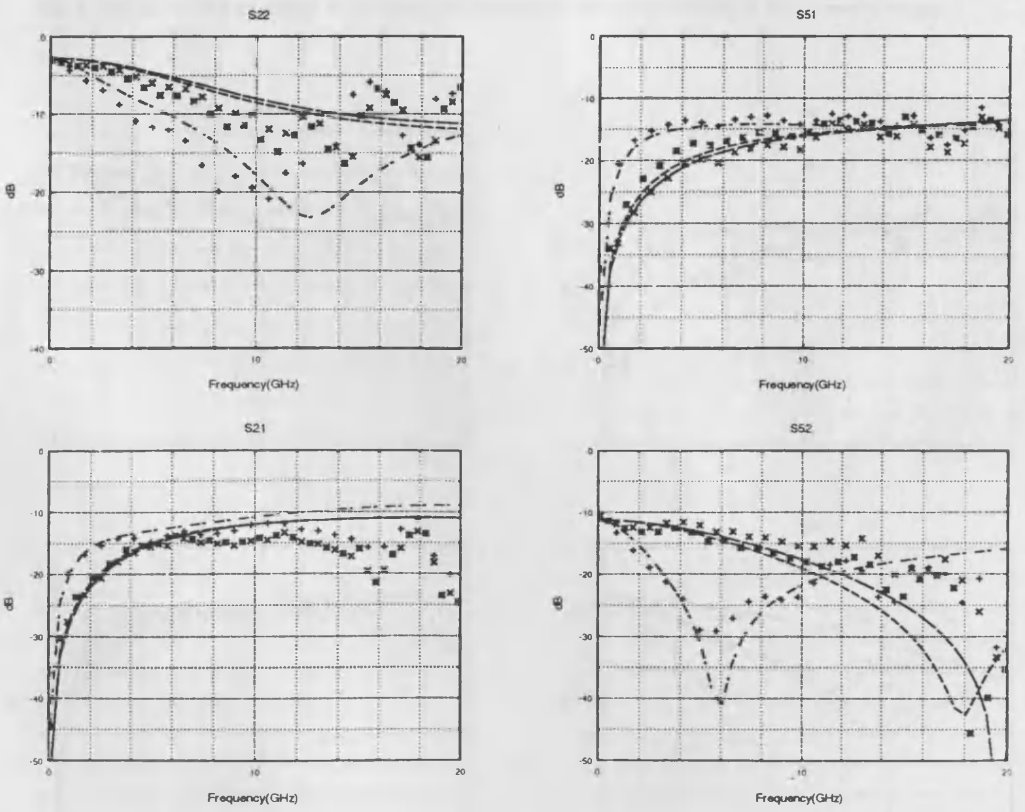

Fig 2. Measured and modelled gate S-parameters for a wide FET with 94μm source length.

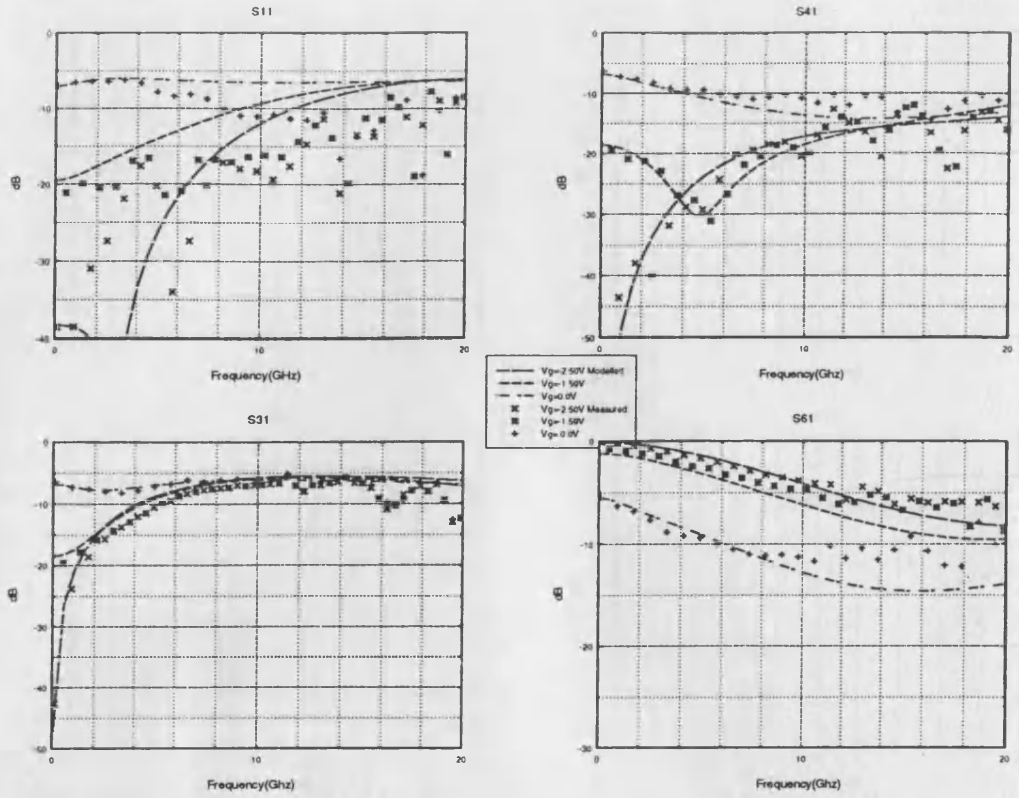

Fig 3. Measured and modelled source-drain S-parameters for a wide FET with 38μm source length.

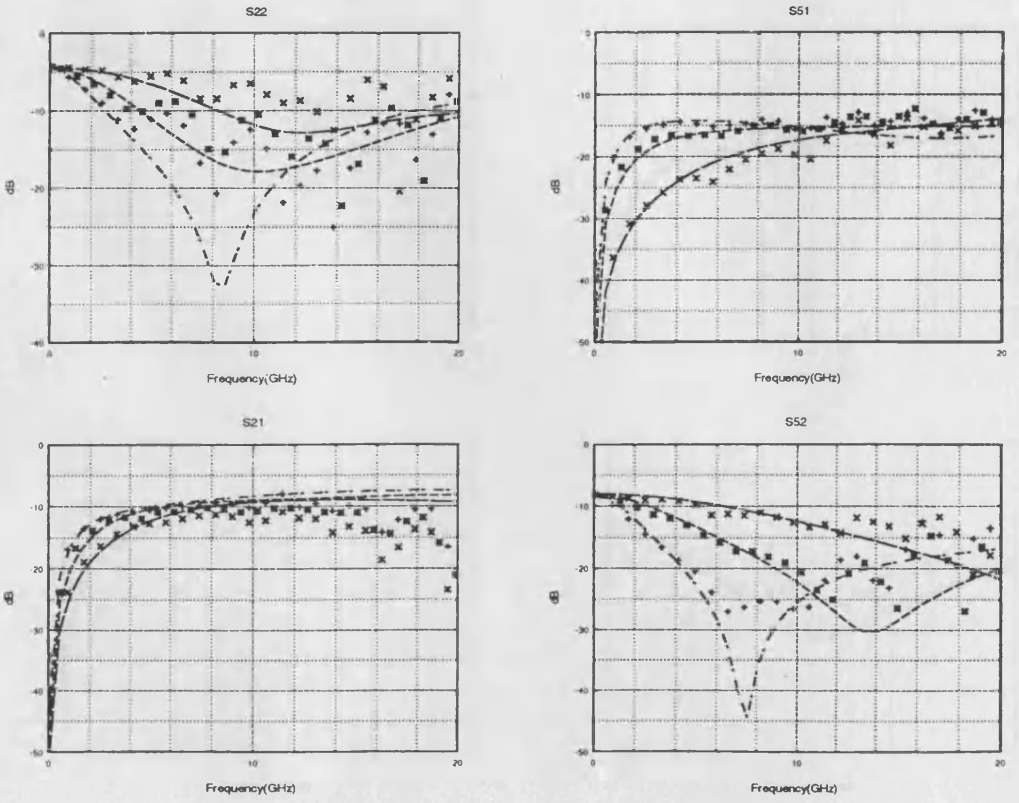

Fig 4. Measured and modelled gate S-parameters for a wide FET with 38μm source length.

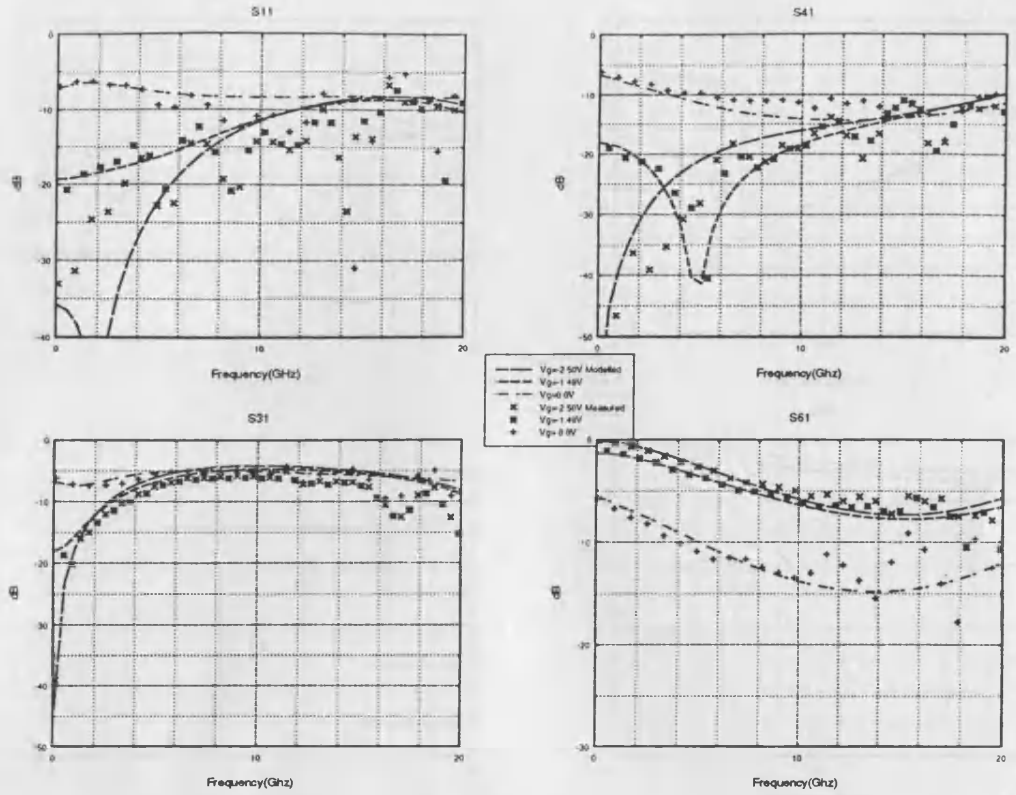

Fig 5. Measured and modelled source-drain S-parameters for a wide FET with 22μm source length.

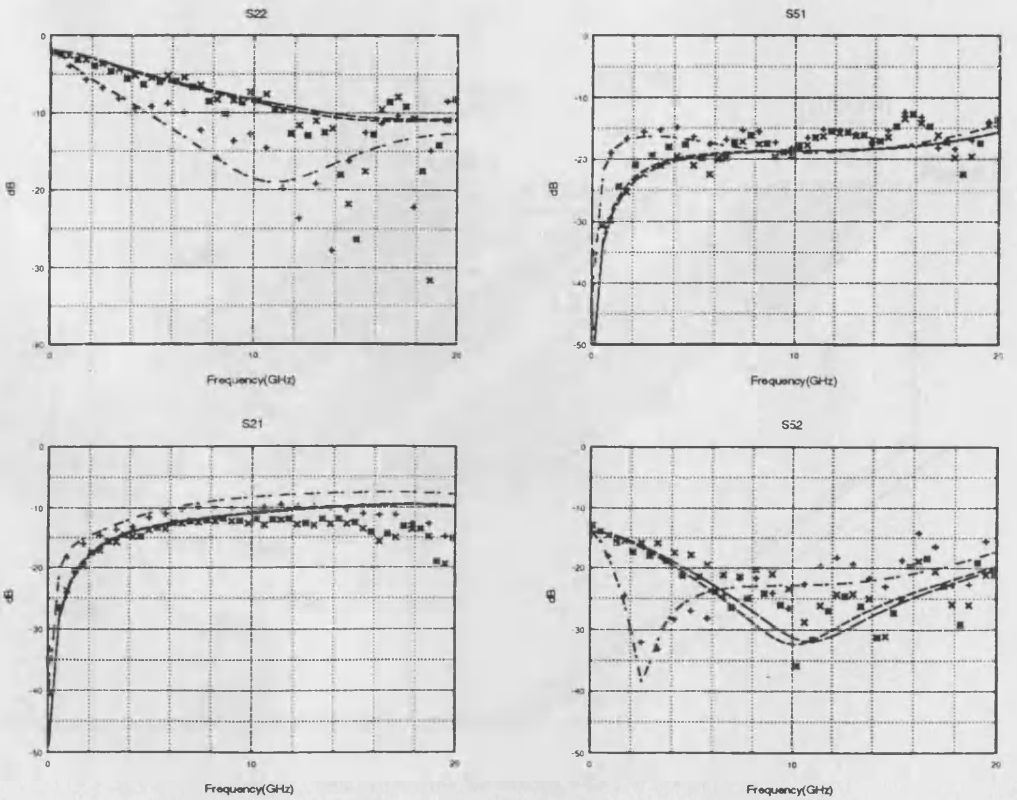

Fig 6. Measured and modelled gate S-parameters for a wide FET with 22μm source length.

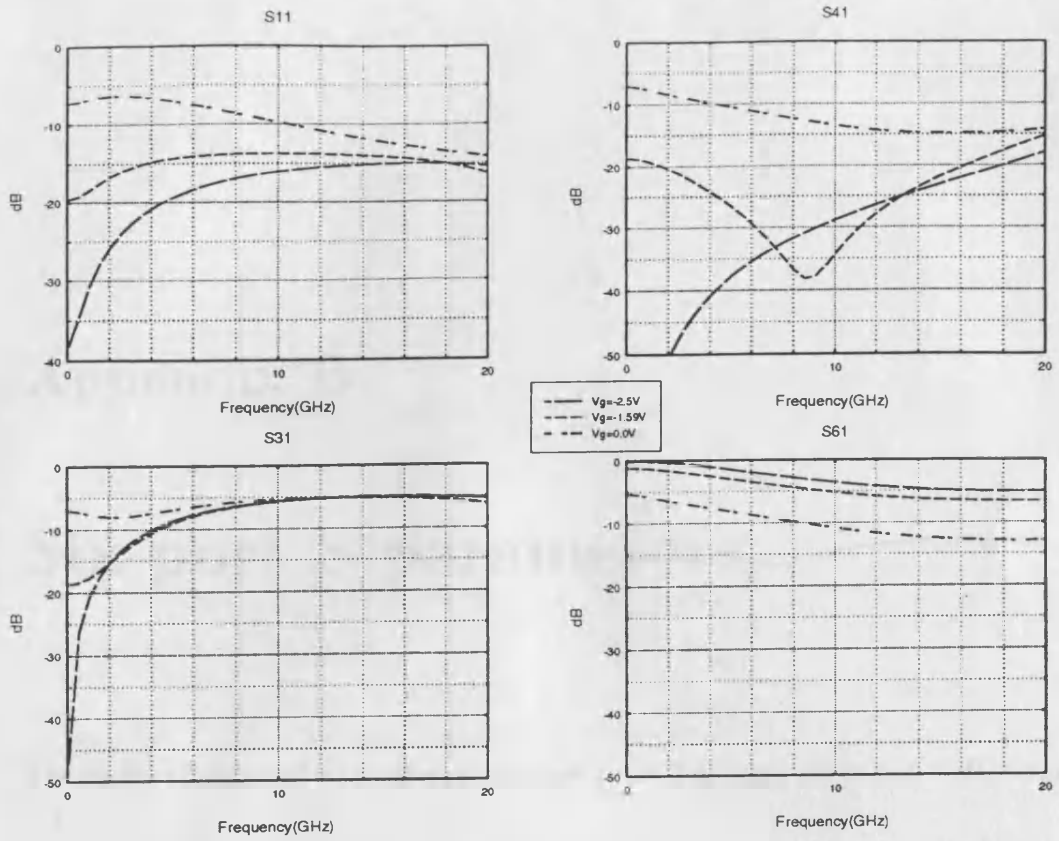

Fig 7. Modelled source-drain S-parameters for a wide FET with 38μm source length and low inductance L=0.05nH connections.

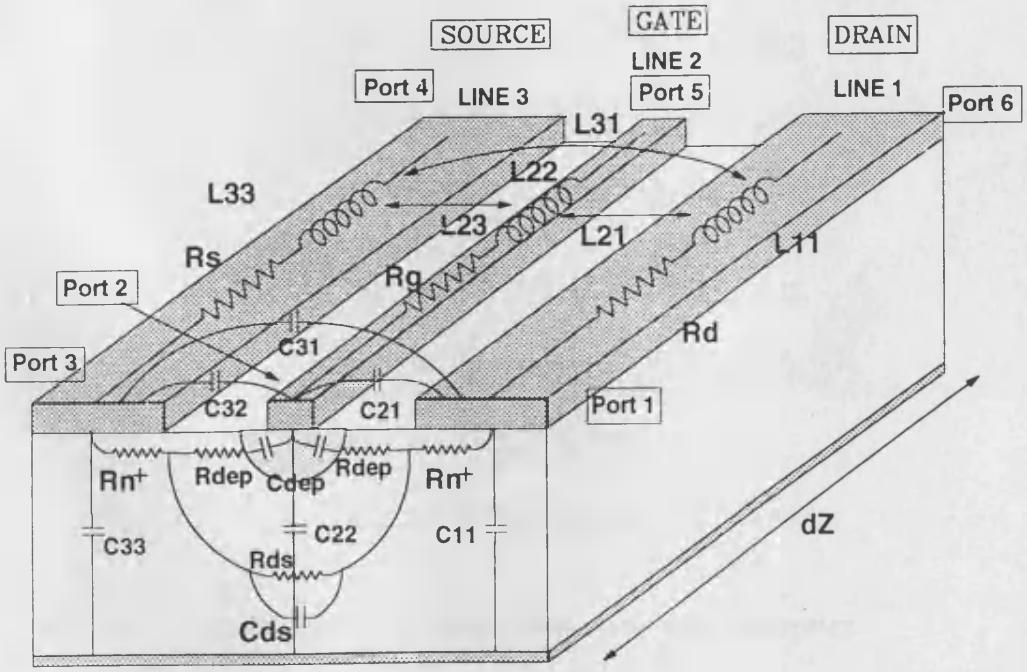

Fig 8. Unit cell for the distributed model of a FET.

Appendix B

Six-port S-parameters

The six port S-parameters for the case of lines 1 and 3 of equal width and NMC terminations are

$$
\begin{aligned}
S_{11} &= \frac{\Gamma_a}{2} - \frac{R_{vc}}{2(R_{vb}-R_{vc})}\Gamma_b + \frac{R_{vb}}{2(R_{vb}-R_{vc})}\Gamma_c \\
S_{21} &= (\Gamma_b - \Gamma_c)\sqrt{\frac{-R_{vb}R_{vc}}{2}}\frac{1}{(R_{vb}-R_{vc})} \\
S_{31} &= -\frac{\Gamma_a}{2} + \frac{(-R_{vc}\Gamma_b+R_{vb}\Gamma_c)}{2(R_{vb}-R_{vc})} \\
S_{41} &= -\frac{T_a}{2} + \frac{(-R_{vc}T_b+R_{vb}T_c)}{2(R_{vb}-R_{vc})} \\
S_{51} &= (T_b - T_c)\sqrt{\frac{-R_{vb}R_{vc}}{2}}\frac{1}{(R_{vb}-R_{vc})} \\
S_{61} &= \frac{T_a}{2} - \frac{R_{vc}}{2(R_{vb}-R_{vc})}T_b + \frac{R_{vb}}{2(R_{vb}-R_{vc})}T_c \\
S_{22} &= \frac{(-R_{vc}\Gamma_c+R_{vb}\Gamma_b)}{2(R_{vb}-R_{vc})} \\
S_{52} &= \frac{(-R_{vc}T_c+R_{vb}T_b)}{2(R_{vb}-R_{vc})}
\end{aligned}
\tag{B.1}
$$

All other S-parameters can be derived from these using symmetry.

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